

Integrated Circuits for Near-infrared Biomedical Signal Acquisition

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“Trust in the LORD with all your heart and lean not on your own understanding; in all your ways acknowledge him, and he will make your paths straight.”

Proverbs 3:5-6

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Integrated Circuits for Near-Infrared Biomedical Signal Acquisition

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ABSTRACT

The effective monitoring of blood pressure is essential to the prevention of hypertension due to aging population. This gives rise to the urge for the development of wearable devices to meet the huge potential need in healthcare products. However, the traditional medical devices such as sphygmomanometer are noisy, bulky, and requiring healthcare personnel to operate. To that end, miniaturization is required if portable device is to be developed. This research centers on the design of analog front-end integrated circuits for bio-medical signal acquisition with near-infrared (NIR) optical sensing. The key challenges include integration of large value components for low frequency operation, robust rejection of DC photocurrent due to variation of physiological condition and LED operating mode, and low power consumption for long battery time.

To meet these challenges, a new NIR sensing system, consisting of a transimpedance amplifier (TIA) and an ultra-low cutoff frequency lowpass filter, is proposed for application in photoplethysmography (PPG) signal acquisition. Light source is pulsed to reduce power consumption. Robust DC rejection for the pulsed signal source is achieved through a sample-and-hold stage in the feed-forward signal path and an error amplifier in the feedback path with an off-chip compensation capacitor. Ultra-low cutoff frequency of the filter is achieved with a new technique that incorporates a pair of current steering transistors that effectively increases the filter capacitance. The design was realized in 0.35- μm CMOS technology. It consumes 600- μW at 2.5-V, and achieves lower-band and upper-band $f_{-3\text{dB}}$ cutoff of 0.46-Hz to 2.8-Hz, respectively.

To achieve full integration and versatility, a dual-loop TIA with DC photocurrent rejection for continuous-time multi-parameter processing is developed. It consists of a pole location control block to push the lower -3dB cutoff frequency to a low

frequency location and a self-regulated DC photocurrent rejection loop to sense the DC current from the photodiode and to perform DC current cancellation. Implemented in 0.35- μm CMOS technology, the chip consumes 155.8- μW from a 2.5-V supplies at I_{dc} of 20- μA . Experimental results show that the circuit can reject a DC current ranging from 2.7- μA to 110- μA , and achieve a tunable lower -3dB cutoff frequency ranging from 0.47-Hz to 370-Hz without using any external components, which corresponds to a 444 times reduction in capacitor size.

近紅外生物醫學信號採集集成電路

全球人口老齡化趨勢的加重使得高血壓的防治工作變得更為嚴峻，有效的血壓監測對於高血壓防治有著相當重要的作用。傳統的醫療設備如水銀血壓計等的使用存在著諸多缺點，包括有噪聲、體積較大、需要專業健康護理人員的操作等，因此，開發穿戴式醫療設備以滿足社會對於保健產品的巨大需求得到了格外的關注。小型化對於便攜式設備的開發是尤為必要的。本研究集中設計用近紅外光學傳感技術採集生物醫學信號的前端模擬集成電路。電路將工作於低頻範圍內，要有效抑制源于生理狀態變動和發光二極管工作模式的直流光電流，並低功耗工作以提供長時供電，這些特徵要求電路使用諸多大標值的元件，如何有效集成這些元件構成本研究的主要技術難點。

為了解決上述技術難題，本論文將介紹一種新型的用於光電容積描記信號採集的近紅外傳感系統，系統包括一個跨阻放大器和一個超低截止頻率的低通濾波器。系統的光源工作於脈衝方式以減少功耗，同時，由一個前饋信號通路中的採樣-保持電路模塊及反饋回路內一個誤差放大電路的片外補償電容來實現脈衝信號源下直流成分的有效抑制。新型基於一對電流舵晶體管的電路能夠有效提高濾波器的電容，進而實現擁有超低截止頻率的低通濾波器。該設計由 0.35 微米 CMOS 技術實現，電路在 2.5 伏工作電壓下功耗為 600 微瓦，濾波器的低頻帶和高頻帶-3dB 截止頻率分別為 0.46Hz 和 2.8Hz。

為了充分體現集成化和多用途功能，本論文同時介紹了一個具有直流光電流抑制功能用於連續多參數處理的雙環跨阻放大器，其包含一個能夠將低頻截止頻率推向更低位置的極點位置控制模塊，和一個能夠自調節直流光電流的回路，該回路感應光電二極管的直流電流，並執行直流電流抑制功能。該芯片由 0.35 微米 CMOS 技術實現，在 2.5 伏電壓供給和 20 微安直流電流下，功耗為 155.8 微瓦。實驗結果表明，該電路能夠有效抑制從 2.7 微安到 110 微安的直流電流，並且能夠在不使用任何外接元件的情況下，實現低頻截止頻率可調的功能，調節範圍在 0.47Hz 到 370Hz，相當於減小電容尺寸近 444 倍。

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CHAPTER 1: INTRODUCTION

1.1 Background

Near-infrared (NIR) sensing has become one of the popular techniques for the acquisition of biomedical signals due to distinctive spectral absorption characteristics of various molecules and soft tissues of human body in the near-infrared spectral region.

Photoplethysmogram (PPG) is a pulse sensing technique that is used to measure arterial pulse waveform from either arterial wall deflection or force at the surface of the skin above a palpable vessel. It is a volume sensing (as opposed to pressure sensing) technique that relies on changes in arterial blood volume that are associated with cardiac contraction, which results in photon absorption and reflection by tissue or hemoglobin when the tip of the index finger is placed into contact with an NIR sensor [1]. Thus, PPG, together with electrocardiogram (ECG), can be used in the measurement and computation of various vital signs such as blood pressure (BP) and SpO_2 [1]-[4] using pulse transit time (PTT) [5]. This is illustrated in Fig. 1.1.

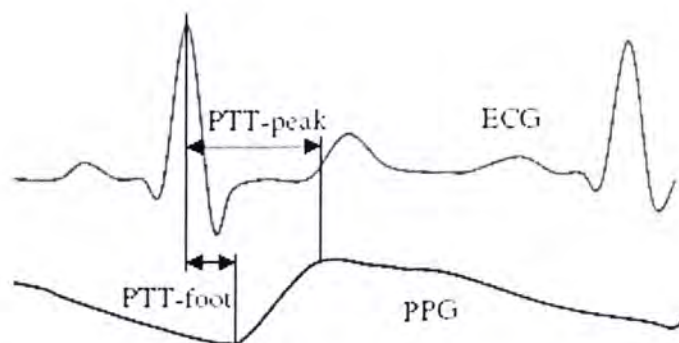


Fig. 1.1 Definition of PTT. (Artwork: courtesy of Ms. Mico Wong, The Chinese University of Hong Kong)

1.2 Motivation

Hypertension is defined as an average systolic blood pressure of 140 mm Hg or greater, a diastolic blood pressure of 90 mm Hg or greater, or the use of antihypertensive medication. According to Kearney *et al.*, the estimated total number of adults in the world with hypertension in 2000 was 972 million. This number was predicted to increase by about 60% to a total of 1.56 billion by 2025 [6]. For this

reason, effective monitoring of BP is essential to the prevention of hypertension. This also gives rise to the urgency for developing wearable medical devices to meet the huge potential need in healthcare products. However, the traditional BP measurement devices such as sphygmomanometer are noisy, bulky, and requiring healthcare personnel to operate. Such device also fails to provide continuous-time monitoring due to periodic cuff inflation and deflation, which causes discomfort to the individual. Frequent occlusion of arteries also induces measurement error [2]. Therefore, a cuff-less, user-friendly, and portable BP measurement device is needed if continuous-time monitoring of vital signs is to be achieved. To that end, Chan *et al.* came up with a BP estimation algorithm, which was based on PTT, using ECG and PPG [2]. The interface for signal acquisitions was built using discrete components, metal lead and NIR sensor, which was also bulky and consumed considerable amount of power. Therefore, an integrated circuit (IC) for the PPG and ECG analog front-end (AFE) is desirable if wearable health monitoring device is to be developed.

However, the current IC development is geared toward high frequency and power system for data communications and heavy duty computing, such as transceiver, microprocessor and analog-to-digital converter (ADC). The design issues for these high frequency front-ends are very different from their low frequency counterpart, which is characterized by slow varying nature of the physiological signal such as PPG and ECG, the physiological condition of the individual, and the stringent power consumption requirement due to its operating conditions.

To illustrate the point, let us take PPG AFE as an example. The signal chain is shown in Fig. 1.2. Since transimpedance amplifier (TIA) in many wireless optical receivers is geared toward high speed, the stability of the TIA must be guaranteed at such a high frequency due to the poles and zero location of the amplifier [7]. On the other hand, TIA can also be employed in biomedical electronics for the acquisition of PPG signal. The photons reflected from molecules and soft tissues in human body experiences loss before reaching a photodiode at the far end. The photodiode then transforms the photons to a proportional current, which is subsequently amplified and converted to voltage by the TIA. In addition, the biomedical signal possesses an inherent DC offset current (I_{dc} – which is not known in advance) due to the following: 1) physiological condition of individual, which varies from person to person, assuming LED is at full power and continuous time operation, 2) duty cycle of the

LED, if it is pulsed to reduce power and 3) the power consumption of the LED in continuous time operation. The ratio of I_{ac} / I_{dc} is given by the following equation:

$$\left(\frac{I_{ac}}{I_{dc}}\right)_{R,IR} \approx \log\left(\frac{\Gamma_{sys}}{\Gamma_{dias}}\right)_{R,IR}$$

which is typically in the range of 0.001 to 0.015 [8]. Since I_{ac} is in the range of 50-nA to few hundred nanoamperes, I_{dc} is in the range of 1-μA to 120-μA. Therefore, the TIA in biomedical electronic must reject this DC component to prevent saturation of signal at later stages, which is different from DC rejection capability for conventional TIA (with operating frequency from 100 KHz to 60 MHz).

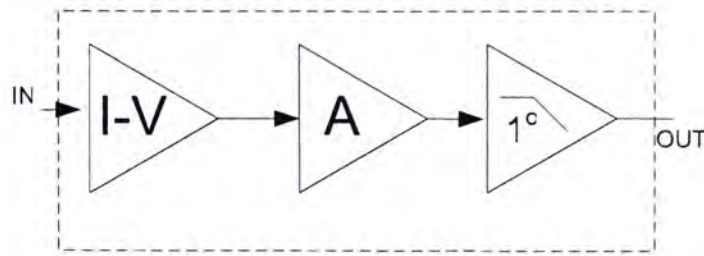


Fig. 1.2 Signal processing chain for PPG AFE.

The DC rejection problem is further complicated when the light source, i.e., the NIR light-emitting diode (LED), is pulsed for reducing power consumption [9]-[10]. The DC level of a pulsed signal is not the same as the DC level of the original continuous-time signal, and depends on the duty cycle of the pulsating scheme. A proper DC rejection should reject the latter rather than the former for maximizing the dynamic range of the system. This is illustrated in Fig. 1.3.

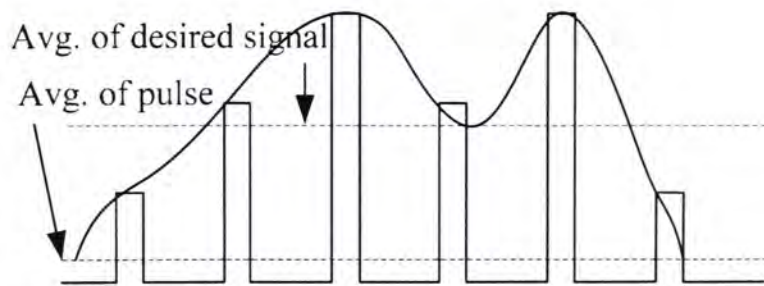


Fig. 1.3 Waveforms to illustrate the difference between the average level of a continuous time signal and the average of a pulse.

Another challenge for the monolithic integration of biomedical front-end is the realization of lowpass filter that requires large RC time constants to remove high frequency noise such as motion artifact in physiological signal, which is of low frequency in nature (0.5 Hz to 4 Hz for PPG). But realization of bulky passive components in silicon is very costly due to its area. Alternatively, low power

consumption stems from the portable nature of the sensor system and the constraint of the power source. This is especially crucial for future design when integrated wireless transmitters are used.

To sum up, these are the challenges that need to be resolved if portable PPG front-end is to be developed: 1) low power consumption, 2) robust DC photocurrent rejection, and 3) integration of large value monolithic passive components. Since there has only been a few reported design of bio-optical signal acquisition circuit [11]-[12], the three aforementioned requirements will provide an interesting application of how IC design techniques can be innovated at both the system and transistor level to address these stringent requirements in the design of PPG AFE.

1.3 Summary of Contributions and Thesis outline

This thesis constitutes a thorough study of PPG signal processing chain to address the requirements placed on the biomedical front-end. The operating frequency of the system is between few tenths of a hertz to a few kilo-hertz, which is reasonable for most physiological signals. In the process of developing the AFE, a graphical method of circuit analysis based upon driving-point impedances (DPI) and signal-flow graphs (SFG) [13], [14] are used.

The following are the main contributions of the thesis:

- a new TIA with adaptive DC photocurrent rejection for pulsed light source,
- an ultra-low frequency lowpass filter using current steering technique,
- a bio-optical signal acquisition front-end for PPG using the new TIA for pulsed light source and the ultra-low frequency lowpass filter, and
- a novel topology for a fully integrated, versatile TIA with adaptive DC photocurrent rejection and very low lower -3dB cutoff frequency.

In Chapter 2, different sensing architectures and techniques for ultra low cutoff frequency filter are evaluated and the proposed architecture and solutions are presented for features comparison. A fully integrated TIA that combines various analog front-end (AFE) of different natures is presented as well. Chapter 3 emphasizes on the design of proposed architectures in Chapter 2: 1) the new transimpedance amplifier for a pulsed LED source and 2) a dual-loop TIA with DC

photocurrent rejection using DPI and SFG. Simulation and experimental results are included within the chapter also. Chapter 4 presents the design and experimental results of ultra low cutoff frequency filter using current steering technique, together with the performance results of the overall system. Finally, Chapter 5 summarizes the thesis and present direction of future works.

CHAPTER 2: SYSTEM DESIGN AND ARCHITECTURE

This chapter provides the background information necessary that leads to the proposed work, which includes the review of previously reported solutions. This includes transimpedance amplifier and sense amplifier for various imaging and hearing aid systems, and filters using G_m -C with sub-threshold operation, switched-capacitor and capacitance multiplier. The design requirements of the proposed system are illustrated through highlighting the limitations of the previous work. Having explained the circumstance for our work on biomedical TIA and low cutoff frequency filter, the proposed solutions will be described to provide an overview and comparison with previous works.

2.1 Architectural consideration

Recent years have seen increased interest in the research and development of NIR sensing in acquisition of biomedical signals. The ultimate goal is to build wearable device with low-power, fully integrated biomedical AFE. Few researchers in the past have built analog front-end for NIR signal acquisition and sense amplifier application. Each is unique in its way to tackle the challenging issues mentioned in previous chapter, which are reviewed in the following section.

2.1.1 Previous work

Normandin *et al.* come up with a NIR brain imager that uses TIA [10], which is given in Fig. 2.1. The system consists of a TIA, post-amps and a demodulator, which is used to recover the pulsed LED signal, with AC coupling circuit intersperses the system - between the amplifier stages. Besides, the LED in Normandin's system is pulsed to reduce power (as is the case with most of the LEDs in biomedical system, with a duty cycle of about 1 percent to 20 percent). In this setting, since the system operates in open-loop and no mechanism is presented to perform regulation of the DC level of the demodulated signal, the signal might become saturated after amplification and leads to reduction of dynamic range (DR), as illustrated in Fig. 2.2.

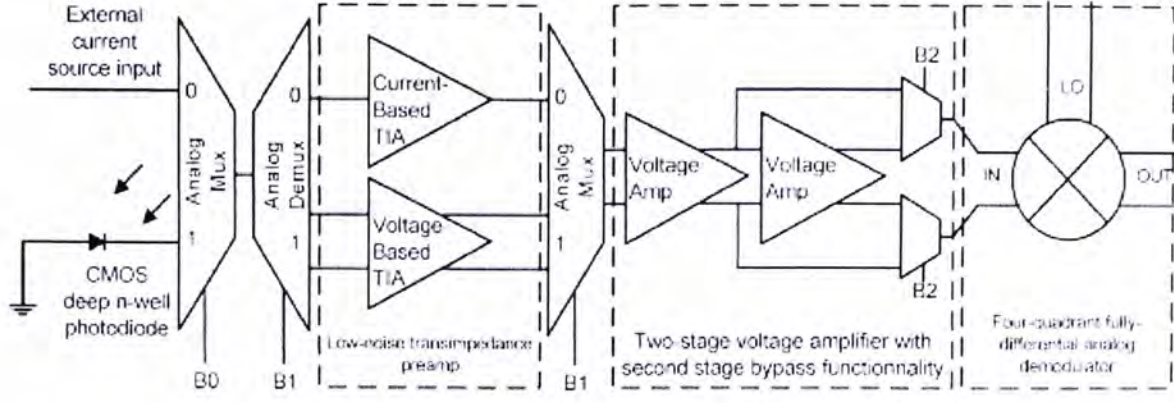


Fig. 2.1 Sensor architecture of Normandin *et al.*, which consists of I-V converter, amplifier and demodulator.

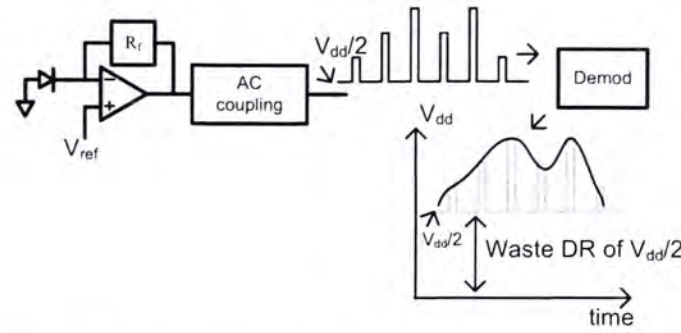


Fig. 2.2 The reduction of DR in Normandin's system.

Additionally, large RC time constant cannot be realized very accurately with the diode-connected transistor in these AC coupling circuits [10], [15] since the component is implemented based on saturation current (I_s) of the transistor, as dictated by Eqs. (2.1) through (2.2):

$$i = I_s e^{\frac{v}{nV_T}} \quad (2.1)$$

$$\frac{\partial i}{\partial v} = I_s e^{\frac{v}{nV_T}} \cdot \frac{1}{nV_T} \quad (2.2)$$

$$\text{where } \frac{1}{g_m} = R = \frac{nV_T}{I_s e^{\frac{v}{nV_T}}}$$

which is largely process and temperature dependent. Since these pseudo resistors are realized using diode-connected configuration, as shown in Fig. 2.3, it exhibits poor linearity and the circuit becomes a rectifier when the signal grows to be larger, which would require a bandpass filter in the subsequent stage for signal extraction. Hence, if a larger gain is desired at the current-to-voltage converter to maximize the signal-to-noise ratio (SNR), the signal would be easily distorted at the AC coupling

circuit. Consequently, this architecture results in reduction of DR because of its building block arrangement, and the transistor level implementation affects the operation of the system at DC.

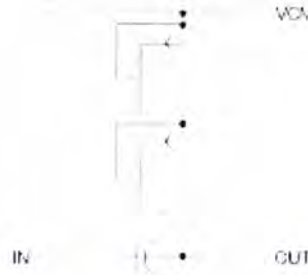


Fig. 2.3 Pseudo-resistor implemented by diode connected transistors.

On the other hand, Baker *et al.* [16] had implemented a microphone amplifier using DC current rejection technique for cochlear implant application. The circuit, shown here in Fig. 2.4, consists of a TIA in forward direction and the G_m block in feedback to sense the voltage across R_f , which in turn controls the microphone output current to be sunk through M_1 . For this application, the focus of this current-to-voltage converter is high power-supply rejection ratio (PSRR) for a *continuous time* audio signal which spans a frequency range of few hundred to few kilohertz; hence, it is unsuitable for the detection of pulsed physiological signal with very low frequency (0.5-Hz to 4-Hz for PPG).

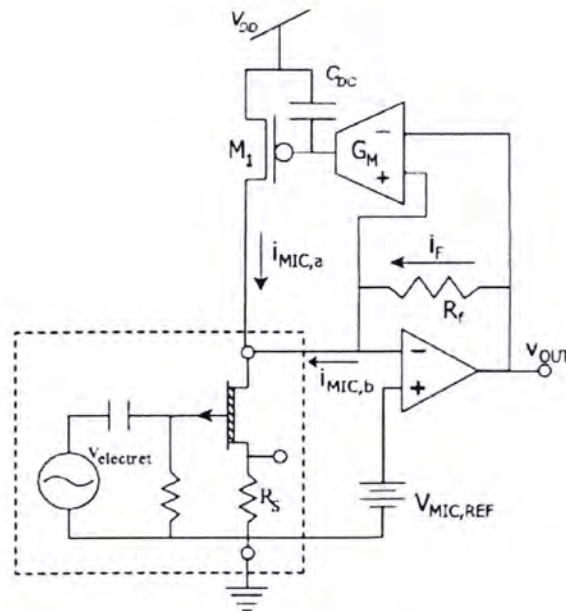


Fig. 2.4 The architecture for the analog front-end of Baker *et al.*, which consists TIA with current cancellation through G_m and M_1 .

Rankov *et al.* [17] and Hayes [18] have also implemented pulse sensing system using correlated double sampling (CDS) for X-ray application, which is shown in Fig.

time-multiplexing the LED, which is pulsed for 1-ms every 10-ms. The input signal is a current pulse being acquired through the PD with AC amplitude of 200 to 300 nA that sits on top of a 50 to 60 μA pulse with f_s of 100-Hz and 10% duty cycle.

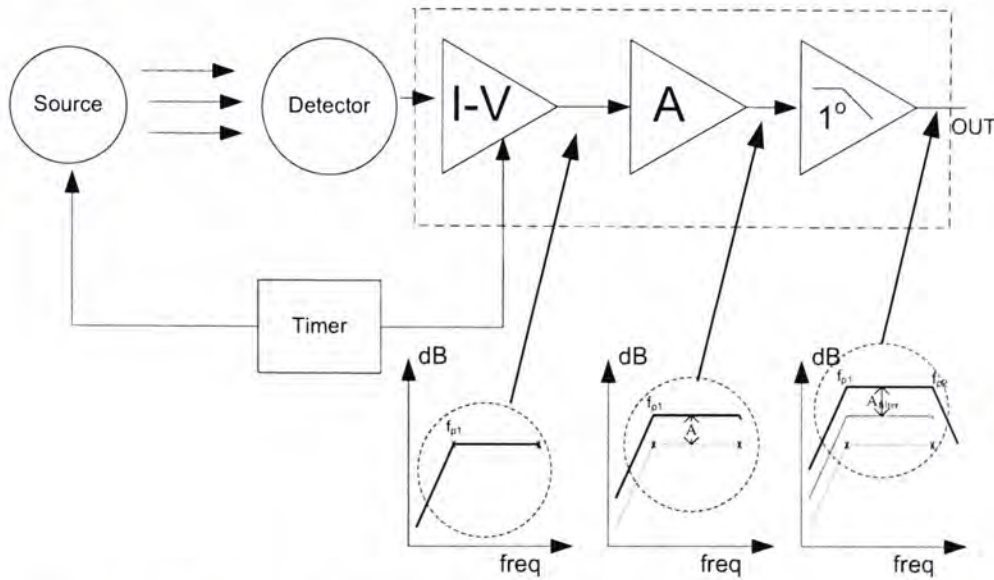


Fig. 2.7 Proposed sensor architecture #1, which consists of a closed-loop TIA, amplifier and current low-pass filter (CS-LPF).

The pulse height is set at 50 to 60 μA because experiments with discrete circuits have shown that DC photocurrent of most subjects spans a range of 60 to 80 μA when physiological signal is acquired through the PD, with the LED fully on. Therefore, with a 10% duty cycle, the actual amount of DC current generated by the PD is about 6-8 μA . This signal is then converted to voltage in the TIA. To detect the average of this pulsating signal accurately, as explained in previous chapter, this pulsed PPG signal is then sampled and held inside the system, together with the feedback mechanism, which will be elaborated in Chapter 3. Finally, smoothing operation is applied to this quantized signal through the CS-LPF and continuous time signal can be recovered for further processing.

The advantage of the system is two-fold: first, unlike the pseudo-resistor AC coupling circuit, the input signal inevitably experiences less distortion with this TIA configuration. Second, the average level of the incoming signal, which is a current pulse, can be computed more accurately through the sample-and-hold (S/H) in the feedback loop circuitry, and current-to-voltage conversion can also be performed simultaneously. Third, since the NIR LED consumes the most power, it needs to be pulsed to reduce power consumption. Inevitably, duty cycle and sampling frequency would affect the accuracy of peak detection algorithm later on for BP estimation [9].

Henceforth, this architecture provides flexibility in duty cycle and sampling frequency selection to optimize for power consumption and BP computation accuracy because it can reject variable amount of DC current. Thus, with proper building block arrangement, the DR of the overall system is not hampered. The compensation in the error amplifier also provides low enough cutoff frequency required to preserve the original signal, as explained in Chapter 3.

B) Dual loop transimpedance amplifier

To build highly miniaturized component for wearable devices, and to combine various front-ends of different natures (but with the same input mode - current) into a single architecture, such as physiological, neural-phonic and hearing-aid signal, there is a need for the development of a fully integrated TIA with DC photocurrent rejection for continuous time application. Fig. 2.8 is the circuit with additional circuitry in the original loop for low frequency operation and another loop for self-regulated DC photocurrent rejection. As will be shown later, the lower-band f_{-3dB} of this circuit is given by the following:

$$\omega_{HP} = \frac{R_f A_{v2} g_{mctl} \frac{g_{m2}}{g_{m1}}}{R_{02} C_m} \quad (2.4)$$

Basically, the AFE consists of two novel parts: 1) a pole location control block that dictates the lower-band f_{-3dB} of the bandpass response with the addition of g_{m2} and $1/g_{m1}$, as shown in Eq. 2.4, and 2) The self-regulated DC photocurrent rejection circuitry, which is consisted of current mirror M_3 to M_8 . The rejection loop senses a wide range of DC current generated by the PD and feedback the current to be cancelled through M_{ctl} such that the power consumption of the LED can be optimized, as seen from previous section. The pole location control block provides flexible lower-band f_{-3dB} (ω_{HP}) selection such that a wide array of input signal can be processed. For instance, the signal bandwidth of the physiological signal (such as PPG and ECG) is from a few tenths of a hertz to few tens of hertz, while neural signal occupies a frequency band from a few hundred hertz to few kilo-hertz. Thus, this front-end must be capable of processing signals with a wide frequency range. With such a complex circuit (no less than three feedback loops that are coupled together) comes

the immense challenge of analyses. Traditional circuit analysis might work, but it will be extremely cumbersome to extract anything useful for design. Therefore, some techniques that can portray the dynamics of the circuit behavior, yet systematic enough to be carried out for analysis, is required. Signal flow graph analysis [13]-[14] has that potential to satisfy the requirement. This will be presented in the latter half of Chapter 3. To conclude, Table 2.1 summarizes the difference among various architectures.

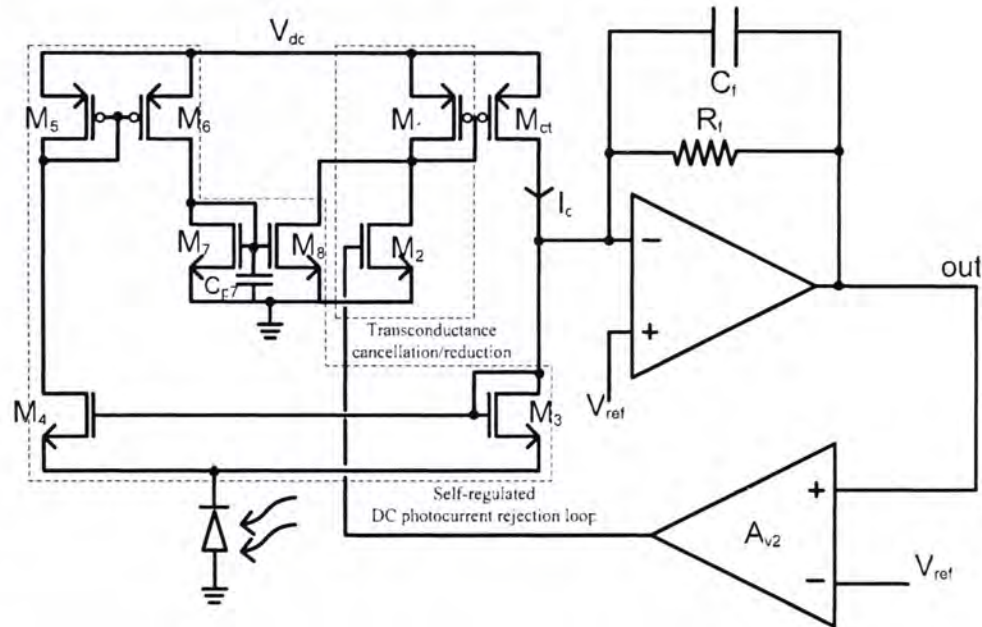


Fig. 2.8 Dual-loop transimpedance amplifier with pole location control block and self-regulated DC photocurrent rejection loop.

2.2 Design consideration for the ultra low cutoff frequency filter

Filter is an important building block for signal processing, whether it is for wireless communications to suppress the interferer or for quantizing signal within a sigma-delta modulator. It can be found in a variety of mixed-signal systems for various purposes. The requirement of the building block varies from application to application and each has its unique properties and design challenges.

For physiological signal processing, since the signal (ECG and PPG) is slow varying in nature (0.5 to 4 beats per second), filter with high cutoff frequency would not work since low frequency noise, such as motion artifact, and charge leakage from S/H, which are in the range of a 10-Hz to 100-Hz, would inevitably distort the small magnitude signal of interest. Therefore, filter with ultra low cutoff frequency is necessary. Nonetheless, implementation of large RC time constant on silicon is very

costly due to area occupied by passive component and is extremely inaccurate due to process variation. In the past, few design techniques have been developed to deal with the issue and they are presented in the following section.

2.2.1 Previous work on very low cutoff frequency filter

A) G_m -C with current division and sub-threshold operation

Figs. 2.9 and 2.10 are the schematic of a transconductor using current division principles and the system architecture for the filter [22]. Basically, M_R in Fig. 2.9 acts as linear transconductor to convert the differential voltage ($v_1 - v_2$) to current and current cancellation is performed at the transconductor output by M_1 and M_N , as shown in the following equation:

$$g_m = \frac{i_o}{v_1 - v_2} = \frac{N - 1}{M + N + 1} g_{oMR} \quad (2.5)$$

where M is defined as the ratio of transconductances between M_M and M_1 and N is defined as the ratio of transconductances between M_N and M_1 .

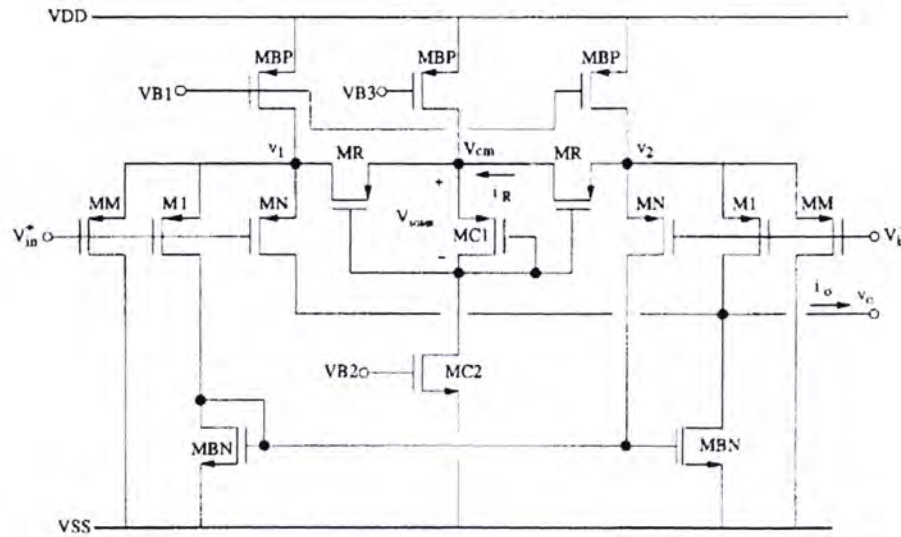


Fig. 2.9 Schematic of transconductor in [22], with current cancellation.

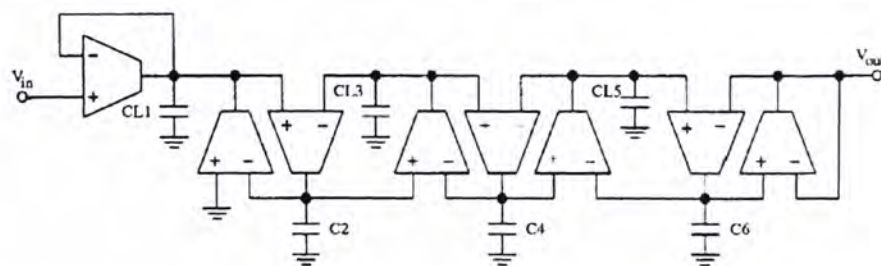


Fig. 2.10 System architecture of the G_m -C filter in [22].

The problem with this circuit is that 1) current cancellation is dependent on the difference of currents flowing through M_1 and M_N , which are operated in sub-threshold regime. Since this difference (not ratio) is process dependent, very small G_m cannot be realized very accurately. 2) In addition, sub-threshold operation in some process is not well controlled, which also contributes to an inaccurate G_m , and 3) the complicated system architecture might give rise to stability problem. To be safe, some other mechanism is necessary to guarantee the required cutoff frequency besides using the transconductor alone. For instance, the pole frequency for a G_m -C filter is given by

$$f_{-3dB} = \frac{g_m}{2\pi C_L} \quad (2.6)$$

From Eq. 2.6, C_L also affects the pole location as well. To be fail-safe, it is necessary to increase the size of the C_L . Capacitance multiplier is the answer and it will be discussed next.

B) Capacitance multiplier

The basic structure of the grounded capacitance multiplier (or grounded impedance scalar) is shown in Fig. 2.11 [22]. Each end of the capacitor is connected to the drain of the current mirror and active load. The current flowing through one branch is amplified and fed back to the input terminal of the capacitor, thus current and capacitance multiplications are achieved. The equivalent input capacitance becomes

$$Z_i = \frac{v_i}{i_i} = \frac{1}{s(N+1)C_i} \quad (2.7)$$

It seems that the capacitance multiplier is an ideal solution to compensate for the inaccurate G_m . Nonetheless, there are drawbacks to this: 1) since the multiplication factor depends on N , therefore, large amount of current is consumed for a large multiplication factor. There is design trade-off between size of capacitor and power consumption. 2) In this topology, the capacitor is parallel with the drain node of the active load and also the current mirror. As a result, the impedance seen by the output of the transconductor is low impedance, which may create loading problem for the G_m block and the high gain of the block might not be maintained. This results in signal attenuation. 3) This technique is only applicable to grounded impedance

scaling and unsuitable for floating impedance scaling, which requires a different circuit. Some modification is required before it is made useful as a versatile impedance scalar.

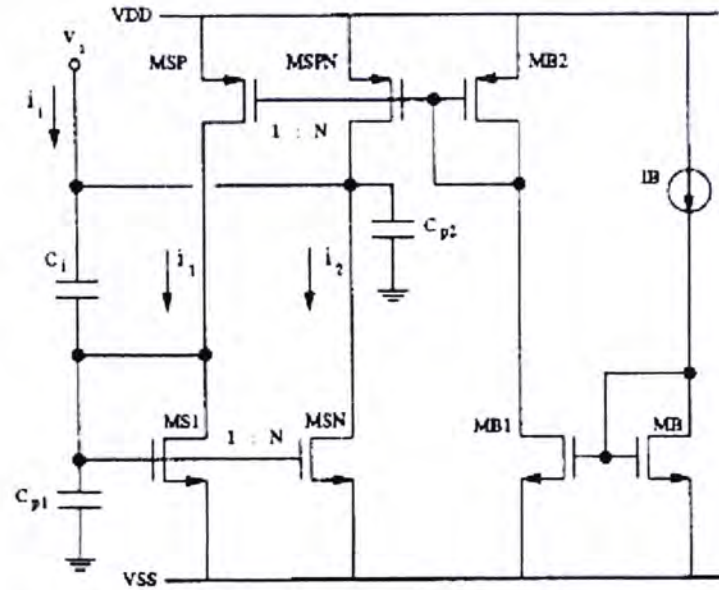


Fig. 2.11 Schematic of impedance scalar in [22].

C) Switched-capacitor (SC) filter and switched-opamp switched-capacitor (SO-SC) filter

The SC-SO filter, presented in Fig. 2.12, is an eighth-order Butterworth bandpass ladder filter being used in [23]. It operates from a 1.8-V to 1-V supply and clocks at 1-KHz. The high sampling rate is required in order to minimize leakage current of the switches due to long hold time, at the price of complexity, larger C_{max} / C_{min} ratio and higher power consumption. The tuning ability of this structure is also limited.

Alternatively, the leakage current cancellation circuit in Fig. 2.13 [24] cancels the leakage current from the CMOS switch such that a smaller C_h can be integrated onto the silicon. However, it is not feasible if such technique is applied to multiple switches, since it would add up in area, power and complexity as well. It also would not work well in low voltage design since four transistors are stacked together.

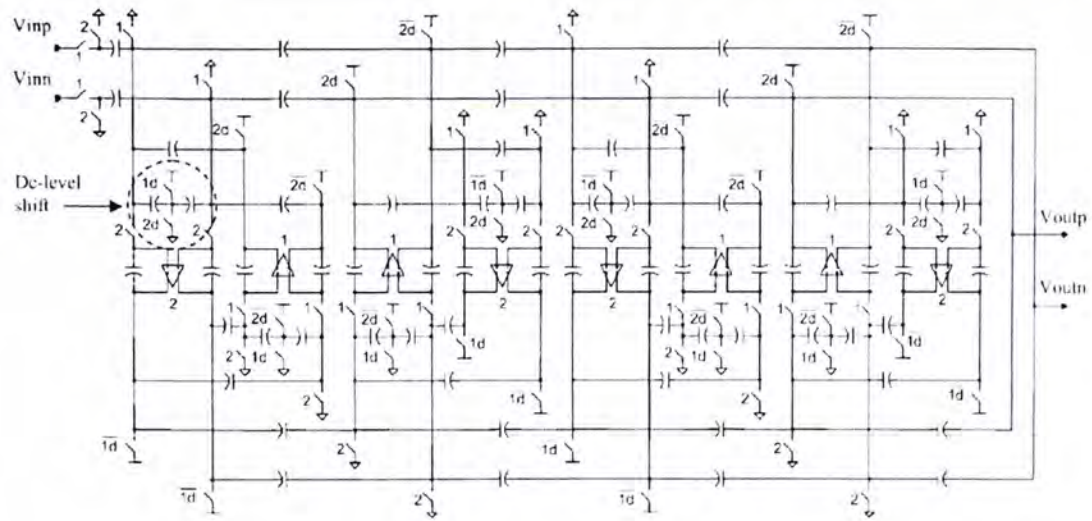


Fig. 2.12 Schematic of SO-SC bandpass filter in [23].

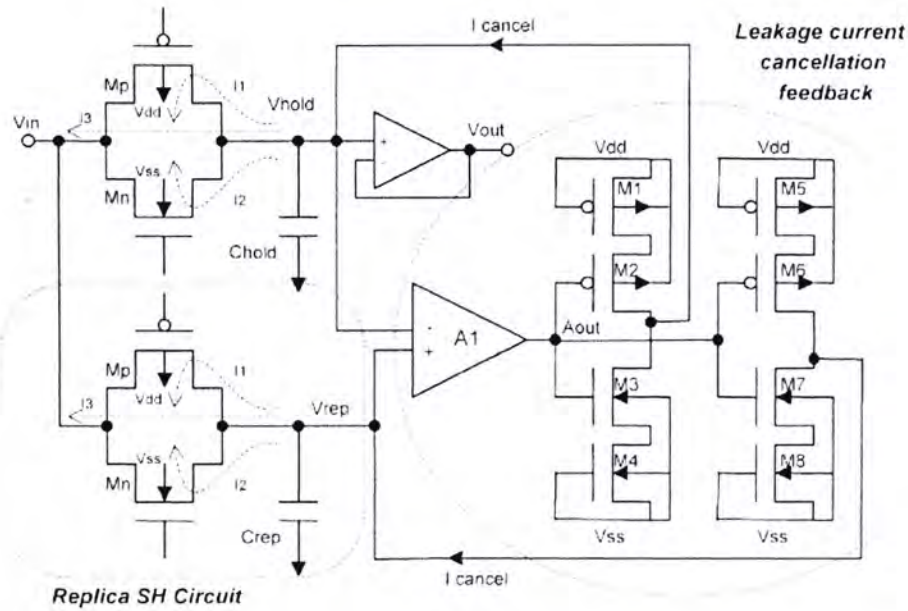


Fig. 2.13 Schematic of the leakage current cancellation circuit in [24].

2.2.2 Proposed work for the ultra low cutoff frequency filter

Current-steering low pass filter (CS-LPF)

To improve the performance of the lowpass filter and address the previous issues, a different structure is purposed in Figs. 2.14a) and b) [21], [25], which is based on Moon [26]. This structure, termed current-steering lowpass filter (CS-LPF), works by varying the gate voltage of the transistor pair inside the α block to steer away certain amount of current to ground from the feedback capacitors in the active RC filters. As a result, the cutoff frequency of the filter can be adjusted. The advantage is multi-faceted. First, current-steering is very simple compared to the SC

or G_m -C technique because it does not require the presence of a clock signal or complex biquad/ladder structure. Thus, there is no switching noise problem, which is usually associated with an SC filter, or stability problem, which is associated with the G_m -C structure. Second, the use of large capacitors can be avoided because of the increasing effective capacitance due to current steering. Third, the process and temperature variation can be compensated for by varying the gate voltage. Although the current steering transistors, which act as linear resistors, might exhibit non-linear behavior, the problem can be minimized by carefully controlling the aspect ratio of the transistors. Accordingly, the advantages far outweigh the drawbacks. Therefore, current-steering technique will be further investigated in later chapter. The filter comparison is summarized in Table 2.2.

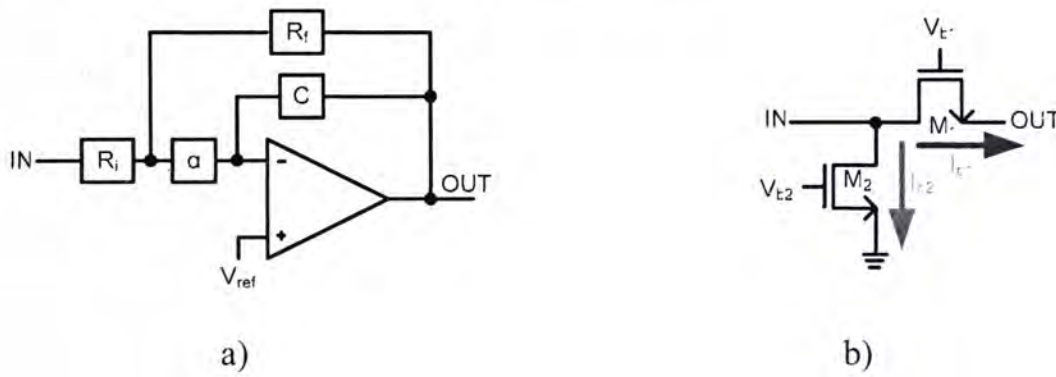


Fig. 2.14 a) Top level of schematic of CS-LPF, and b) schematic of α block.

2.3 Summary

In this chapter, the architectural consideration from the system perspective is presented. Namely, four kinds of architecture are considered: discrete-time neural-phonic signal processing using pseudo-resistor, continuous-time audio frequency signal processing using sense amplifier feedback mechanism, correlated double sampling, and discrete time physiological signal processing using current rejection and sample-and-hold. The feasibility study of different architectures to fulfill the requirements: namely, low-power consumption, robust DC photocurrent rejection and integration of large value monolithic passive components, is conducted. To that end, the proposed discrete time current rejection architecture fulfills the requirement and performs better than the other three.

Next, full integration of the previous architecture and a multi-parameter AFE are accomplished by a dual-loop TIA with DC photocurrent rejection. Not only does this

TIA accomplishes the same feat as the previous architecture, but also it can handle signals arises from different parts of body, such as neural photonic, hearing-aid and physiological signal. To facilitate analysis of the multi-loop circuit, signal flow graph is used to gain insight into the operation and dynamic behavior of the circuit. Thus, the building blocks and the analysis technique will be further investigated in later chapters.

Furthermore, techniques for the design of ultra-low cutoff frequency are evaluated. They are G_m -C with current cancellation and sub-threshold operation, capacitance multiplication and switched-opamp switched-capacitor (SO-SC). They are scrutinized for its f_{-3dB} cutoff accuracy, power consumption, versatility, and structural and implementation complexity. Consequently, the proposed CS-LPF complies with most of the requirement and out-performs the other three. This will be examined in Chapter 4.

Reference	Architecture	Comment
[10], [15]	Open-loop, diode-connected AC coupling, demodulator	<ul style="list-style-type: none"> No regulation of DC level Inaccurate RC time constant Limited linearity
[16]	TIA with DC photocurrent rejection, close-loop for audio signal.	<ul style="list-style-type: none"> For continuous time and audio frequency signal.
[17]-[18]	Correlated double sampling	<ul style="list-style-type: none"> Folding problem. Predetermined offset required.
Proposed work #1	TIA with DC photocurrent rejection, close-loop for discrete time low frequency physiological signal.	<ul style="list-style-type: none"> For discrete time, low frequency physiological signal. Low distortion. Accurate RC time constant.
Proposed work #2	Dual-loop TIA with DC photocurrent rejection, close-loop for continuous time multi-parameter signal.	<ul style="list-style-type: none"> Combining various AFE of different natures into a single architecture. Full integration.

Table 2.1 Summary of different architectures.

Reference	Technique	Comment
[22]	G_m -C with current cancellation and sub-threshold operation	<ul style="list-style-type: none"> Inaccurate G_m Stability problem
[22]	Capacitance multiplier - Impedance scaling with current mirror.	<ul style="list-style-type: none"> Only good for grounded configuration. Trade-off between size of capacitor and power. Loading problem
[23]-[24]	Switched-opamp switched capacitor for low voltage, low power operation. Leakage current cancellation technique	<ul style="list-style-type: none"> Large C_{max} / C_{min} ratio. Leakage current. Limited tuning range Structural complexity Headroom problem
Proposed work #3	Current steering lowpass filter	<ul style="list-style-type: none"> Compensated for process and temperature variation Higher power consumption.

Table 2.2 Summary of different ultra low cutoff frequency design techniques.

CHAPTER 3: TRANSIMPEDANCE AMPLIFIER DESIGN

In this chapter, we work out a number of transimpedance amplifier (TIA) structures that fulfill the requirements mentioned in previous chapters: 1) robust DC photocurrent rejection, 2) reduced lower-band f_{-3dB} and 3) full integration. To that end, we describe in detail a TIA with sample-and-hold (S/H) in feedback to construct a continuous-time voltage output from a discrete-time current input with maximized dynamic range (DR). Next, we develop the topology of a dual-loop TIA with robust DC photocurrent rejection. During the design phase of the dual-loop TIA, we use DPI/SFG to aid us in the analysis of the system. Simulation and implementation results of the proposed designs will be presented as well.

3.1 Transimpedance amplifier with off-chip component

3.1.1 Transimpedance amplifier with DC photocurrent rejection

As mentioned in previous chapters, there is a need for the development of a current-to-voltage converter that can regulate voltage output coming from a pulsed current source [10], [15]. The problem with these circuits is that the DC output voltage cannot be properly detected with a pulsed current or voltage input.

Obviously, a feedback loop with error amplifier (EA) is necessary, such as the one shown in Fig. 3.1 [7]. This circuit performs the following functions: 1) current-to-voltage conversion through R_f of the TIA, 2) DC photocurrent rejection as the error voltage is sensed by EA to determine the amount of DC current to be sunk from the photodiode (PD) through M_{cl} , 3) highpass filtering through the feedback mechanism, which will be explained here, and 4) regulation of DC output voltage to V_{ref} through the use of feedback loop.

The characteristics of the ambient photocurrent rejection circuit can be studied by assuming the gain of the EA – $A_{err}(s)$ has a dominant pole response

$$A_{err}(s) = \frac{A_{dc}}{1 + s / \omega_{p1}} \quad (3.1)$$

where $A_{dc} = g_{mEA} R_{02}$ and g_{mEA} is the transconductance and R_{02} is the output impedance of the EA, respectively. $\omega_{p1} = 1 / (R_{02} C_m)$ is the dominant pole frequency where C_m is the compensation capacitor of the EA. The resulting closed-loop response of the preamplifier with ambient rejection is

$$\frac{v_{out}}{i_s}(s) = \frac{R_f}{1 + L(s)} \approx \frac{1}{A_{dc} g_{mctl}} \times \frac{1 + \frac{s}{\omega_{p1}}}{1 + \frac{s}{R_f A_{dc} \omega_{p1} g_{mctl}}} \quad (3.2)$$

where R_f is the passband gain of the TIA, and g_{mctl} is the transconductance of M_{ctl} . Assuming $R_f A_{dc} \omega_{p1} \gg 1$, the preamplifier exhibits a highpass response with the following lower-band f_{-3dB} :

$$\omega_{HP} = R_f A_{dc} \omega_{p1} g_{mctl} \quad (3.3)$$

It can be seen that this circuit works fine for high frequency operation. Yet, two problems emerge if this circuit is used for low frequency operation with modulation: 1) only very small amount of current can be sunk with a reduced lower-band f_{-3dB} , as seen in Eq. 3.3 unless very large time constant is implemented in the EA for bandwidth extension to reject moderate amount of DC photocurrent, and 2) incorrect average detection for pulsating signal. The first point is relevant because the sunk current is in microampere range regardless of operating frequencies. However, this is not an issue since an external compensation capacitor will be used. Conversely, for a current pulse whose output is a voltage pulse, as the output is integrated by the EA, the offset voltage of the voltage pulse becomes the average. Consequently, output from integration is incorrect and the DC current generated from M_{ctl} is inaccurate. This is acceptable if signal is not being further processed. Otherwise, saturation of signal occurs in later stage due to unregulated DC output voltage being amplified. This is illustrated in Fig. 3.2.

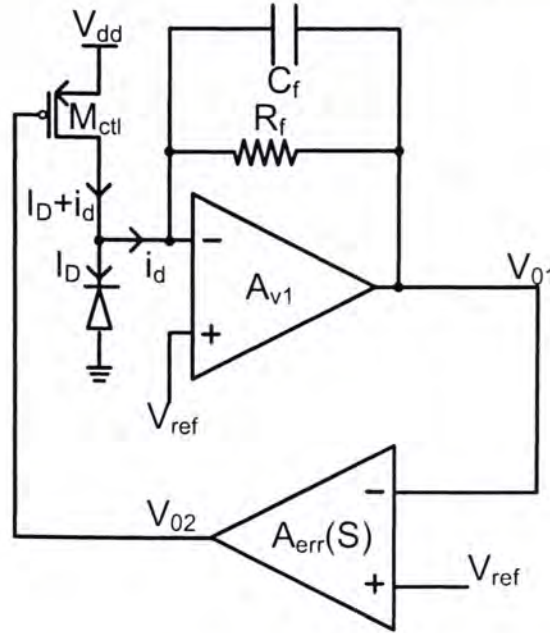


Fig. 3.1 Basic transimpedance amplifier with DC photocurrent rejection [7].

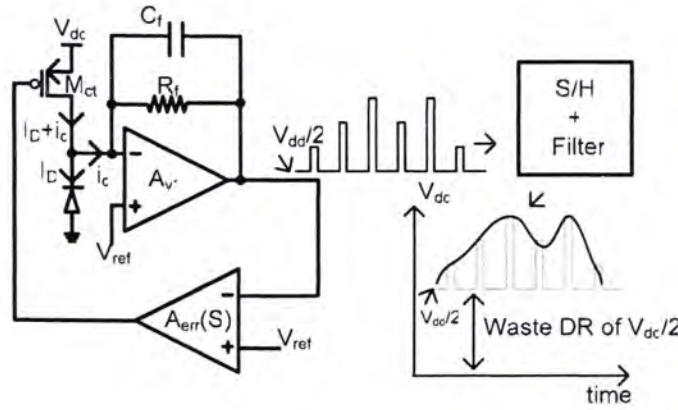


Fig. 3.2 Illustration of how Phang's circuit results in DR reduction.

3.1.2 Proposed solution – Transimpedance amplifier with sample-and-hold in feedback

A) Operating principle

To circumvent the incorrect average detection issue, a different topology in the feedback loop is proposed, which is shown in Fig. 3.3a), b) and c), together with the aspect ratio of the opamps and M_{ctl} . Since the average of continuous-time signal is desired but not the pulse signal, an S/H circuit is inserted between the TIA and the EA. As the current pulses are being converted to voltage pulses through the TIA, instead of integrating the pulsated signal to detect its average, the EA integrates the sampled and held version of the signal such that the average of the signal can be detected accurately. Thus, robust DC photocurrent rejection for a pulsed light source and

accurate detection of DC level of pulsed voltage can be achieved by the addition of one S/H circuit.

To illustrate the point, the system in Fig. 2.7 is designed and implemented in 0.35- μm CMOS technology using a 2.5-V power supply. In this section, only the design issues relevant to the TIA are discussed and the design of lowpass filter will be addressed in Chapter 4. Except for the compensation capacitor (C_m) in the EA, which is 220-nF, and the holding capacitor (C_H) in S/H circuit, which is 10-nF, everything else has been realized on chip. The EA and the TIA opamps are two-stage amplifier in [27]. The use of slightly larger capacitor is to reduce the charge injection such that a larger switch can be used to ensure loop stability. The size of these capacitors can be scaled down substantially in future development by using smaller switch size and capacitor multiplier technique [20], [28]. The gain is R_f and a $2\text{K}\Omega$ resistor is used. The circuit achieves a highpass cutoff frequency of 1-Hz and sufficient amount of attenuation according to Eqs. 3.2 and 3.3.

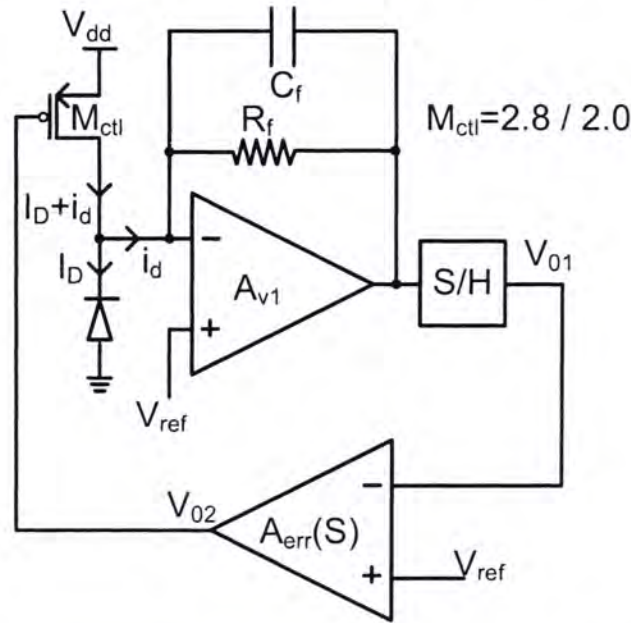


Fig. 3.3a DC photocurrent rejection transimpedance amplifier with sample-and-hold in feedback loop.

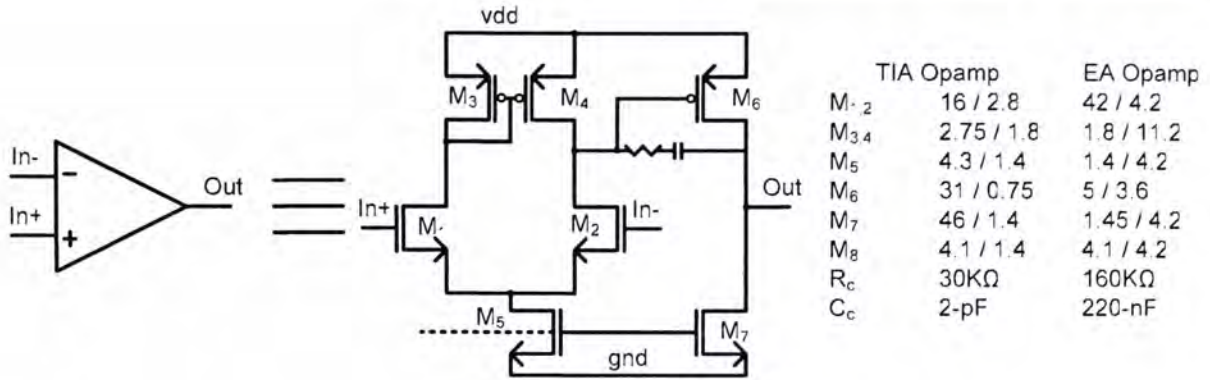


Fig. 3.3b Schematic of opamp, which is taken from [27].

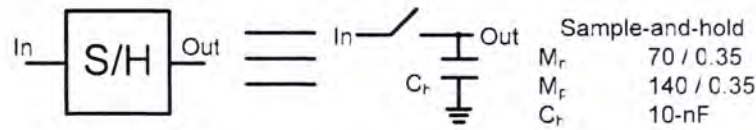


Fig. 3.3c Schematic of the sample-and-hold in Fig. 3.3a.

B) Simulation results

The frequency response of the DC current rejection TIA with EA and S/H in feedback is presented in Fig. 3.4. The circuit achieves 51.2-dB attenuation for a photocurrent of 70- μ A with a lower-band f_{-3dB} of 1-Hz. The range of DC photocurrent that can be sunk effectively while maintaining the desired frequency response is 1- μ A to 70- μ A.

The transient waveform of node V_{out} in Fig. 3.3a is given in Fig. 3.5. The inputs to the TIA are triangular current pulses with a DC photocurrent (I_{dc}) of 1.0- μ A to 70- μ A (0.1- μ A to 7- μ A with 10% duty cycle). When settled, the output DC level equals to V_{ref} , which is at the desired value of $V_{dd} / 2 = 1.25$ -V, given that V_{dd} is 2.5-V. The settling time is about 3.52-s, which is adequate since the circuit operates at very low frequency. The circuit is clearly working as the amount of DC offset is very small for different amounts of DC current.

In Fig. 3.6, the transient waveform for the conventional approach of not placing the S/H inside the feedback loop (circuit in Fig. 3.2) demonstrates that the output DC level varies for different amount of DC photocurrent (from 6- μ A to 95- μ A), from 1.26 to 1.384-V. Clearly, if this signal was further processed (see Fig. 2.7), saturation of DC level would occur at later stage. Consequently, the proposed circuit can remove the DC offset properly and hence increases the DR of the system.

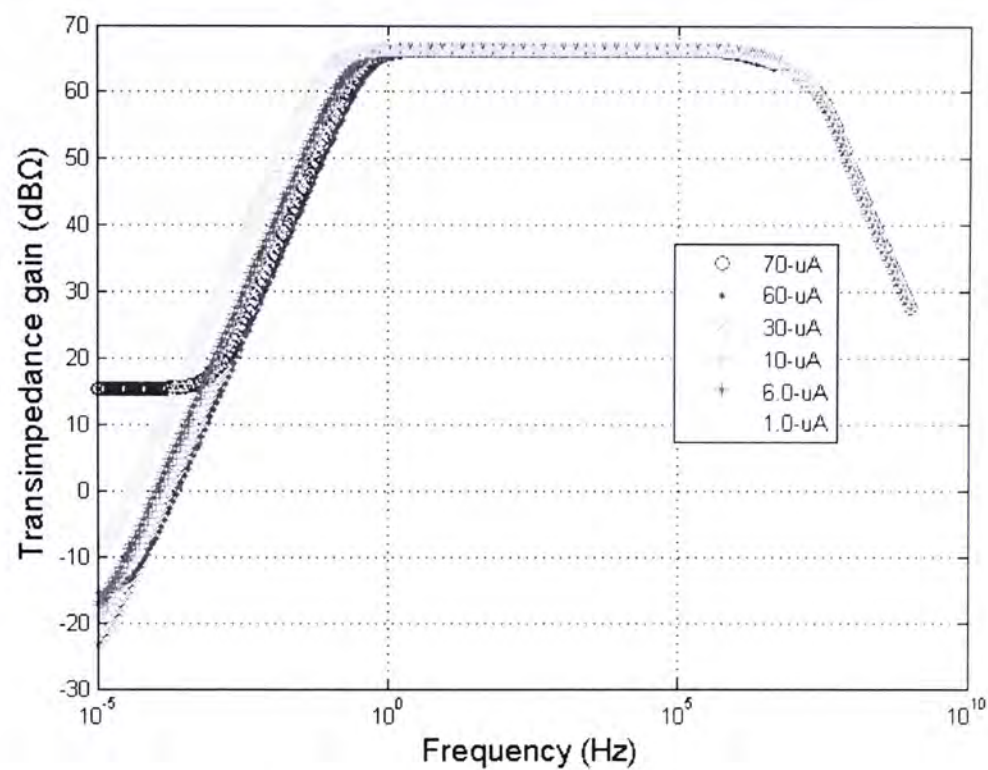


Fig. 3.4 Simulated frequency response of off-chip capacitor TIA with different amount of DC photocurrent

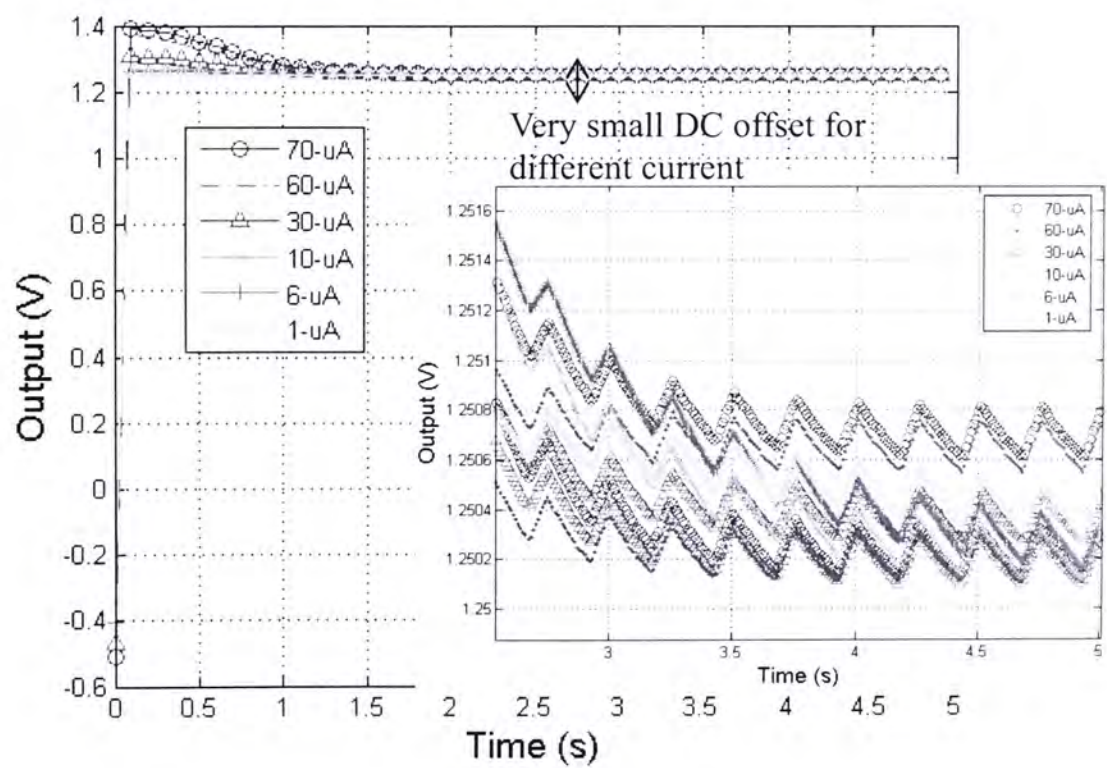


Fig. 3.5 Simulated V_{out} of the TIA with S/H inside the feedback loop with various amounts of DC photocurrent. Inset, zoom-in version of waveforms to show settling within certain range.

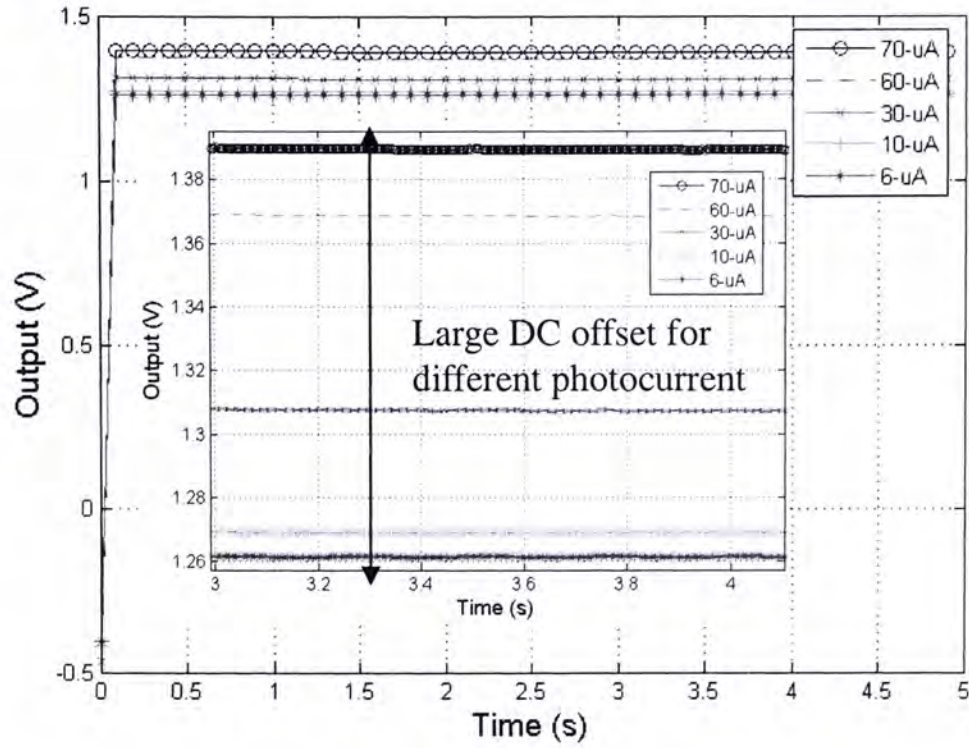


Fig. 3.6 Transient simulation of TIA with S/H outside the feedback loop with various amounts of DC photocurrent. Inset: zoom-in version of waveform to show different amount of offsets.

3.2 Dual-loop transimpedance amplifier with DC photocurrent rejection

3.2.1 Evolution from basics to the proposed work

As mentioned in previous chapters, the main challenges in designing TIA for biomedical application are 1) the integration of large value monolithic components to achieve low frequency operation, and 2) robust DC photocurrent rejection due to variable physiological condition of individuals and reduced LED power consumption for continuous time operation. In this section, the advancement from the rudimentary version of [7] to the proposed work, which overcomes the aforementioned challenges, will be detailed. Afterwards, the analysis and design of the system using SFG will be presented.

Since the operating principles of Fig. 3.1 have been elaborated already in previous section, it will not be repeated here. However, the corresponding lower-band f_{-3dB} is presented again, together with the structure of Fig. 3.1, in Fig. 3.7 (where A_{err} is replaced by A_{v2}):

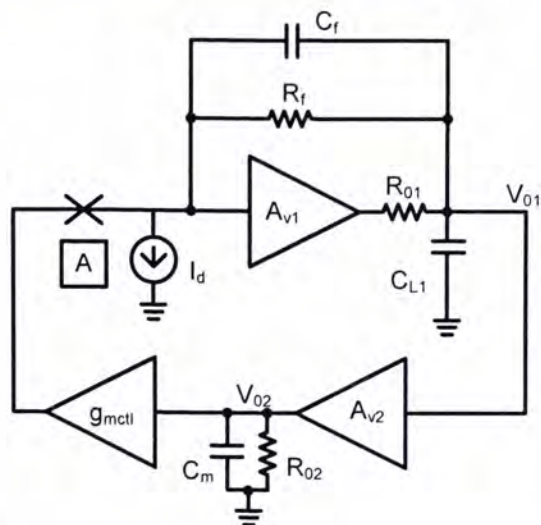


Fig. 3.7 Structure of Phang’s circuit in Fig. 3.1.

$$\omega_{HP} = \frac{R_f A_{v2} g_{mctl}}{R_{02} C_m}$$

The problem with this circuit is that the DC photocurrent that can be sunk at low frequency (< 300 Hz) is low ($< 1 \mu\text{A}$), which is insufficient because PD generates DC current in microampere range ($1\text{-}\mu\text{A}$ to $110\text{-}\mu\text{A}$) regardless of the operating frequency of the circuit [8]. From the above equation, to generate small ω_{HP} (< 300 Hz) with moderate amount of g_{mctl} , the compensation capacitor (C_m) can be quite large. For example, to reach a cutoff frequency of less than 300-Hz and to sink a DC photocurrent of $10\text{-}\mu\text{A}$, even with maximizing the error amplifier’s performance ($A_{v2} = 324.3\text{K-V/V}$, $R_{02} = 161.2 \text{ G}\Omega$), the required C_m is 400-pF . Table 3.1 shows the cutoff frequency and its corresponding C_m .

Cutoff frequency (Hz)	DC photocurrent (μA)	C_m (pF)
300	20	800
300	10	400
50	10	2400
10	10	12000

Table 3.1 Possible values to adapt Phang’s circuit for low frequency application.

To circumvent the problem, the following structure is proposed:

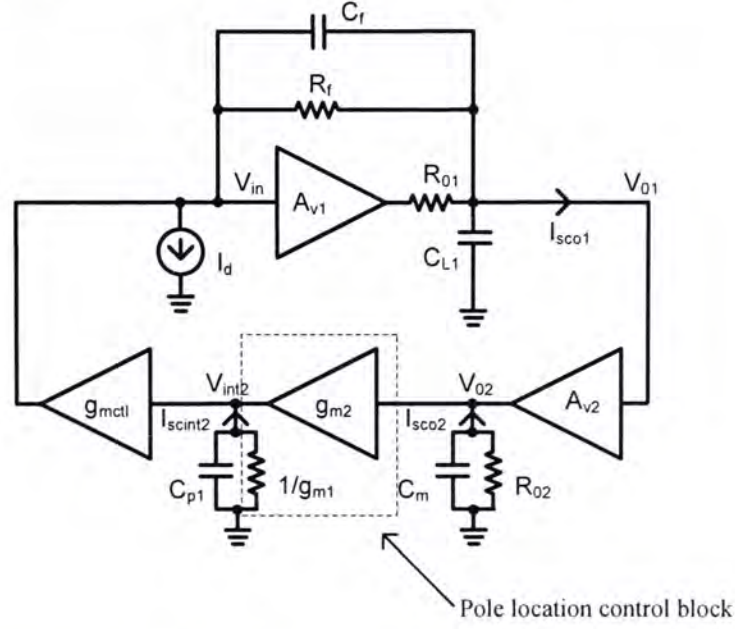


Fig. 3.8 The structure of the new circuit, with transconductance cancellation and reduction blocks (g_{m2} and $1/g_{m1}$) inserted between A_{v2} and g_{mcl} .

In Fig. 3.8, a transconductance block (g_{m2}) and the current-to-voltage block ($1/g_{m1}$) are inserted between the EA and g_{mcl} . The purpose of $1/g_{m1}$ is to cancel with the g_{mcl} such that the lower-band f_{-3dB} is *almost* independent of the current sink function, as shown in Eq. 3.4. However, it will be demonstrated in later section that relationship between g_{m2} and I_{dc} exists which enables the f_{-3dB} to be tuned over a considerable frequency range. Moreover, since g_{m1} cancels with g_{mcl} , there needs to be another transconductance block to feedback current into M_1 from the EA to perform cancellation, and M_2 serves that purpose. Inevitably, g_{m2} has to be kept to a minimum to push the lower-band f_{-3dB} to very low frequency. The following is the new equation for the lower-band f_{-3dB} :

$$\omega_{HP} = \frac{R_f A_{v2} g_{mcl} \frac{g_{m2}}{g_{m1}}}{R_{02} C_m} \quad (3.4)$$

By designing $g_{m2} / g_{m1} \ll 1$, f_{-3dB} can be pushed to an ultra-low frequency that is predictable by (3.4). Moreover, since C_m is large and M_2 is small in size, the AC current from M_2 is negligible and will not affect the rejection of the DC photocurrent. Conversely, according to Eq. 3.4, the design of the EA is crucial in determining the lower-band f_{-3dB} . So sub-threshold operation is required at input diff-pair of the EA to minimize g_m , and R_{02} and C_m have to be maximized to lower ω_{HP} .

The implementation of the above structure is shown below:

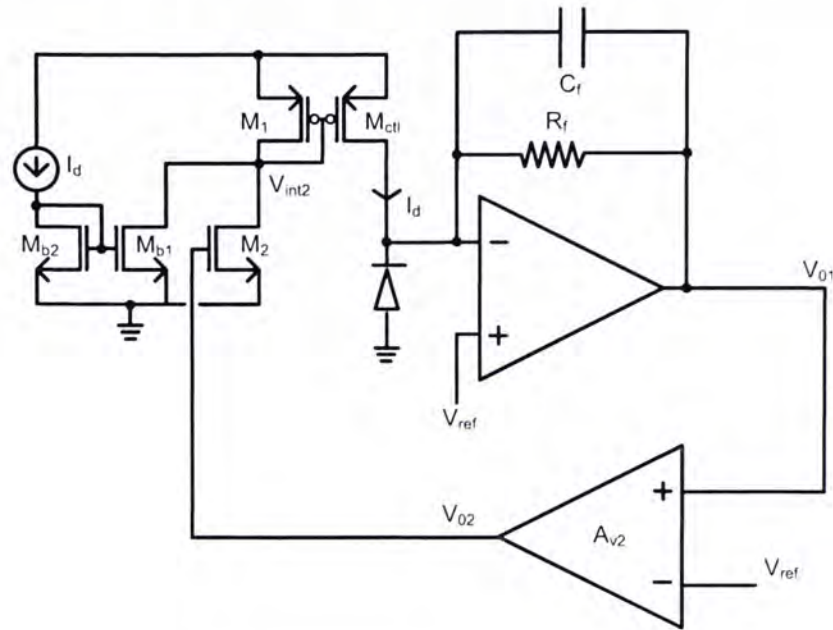


Fig. 3.9 The schematic of the proposed structure in Fig. 3.8.

Here, since g_{m2} has to be kept small to generate the very low frequency pole, the nanoampere current generated by M_2 is insufficient to cancel the original amount of DC photocurrent generated by the PD, which is in microampere range. Hence, I_d is *manually* supplied through the current mirror M_{b1} and M_{b2} , and together with I_{M2} , they are used to cancel the current generated by the PD through the current mirror M_1 and M_{ct1} . However, the major problem with this implementation is that the amount of current to be rejected needs to be known in advance to manually supply the correct I_d . In practice I_d changes according to the power consumed by the LED and in later version, the LED might have to be modulated by various duty cycles (5 percent to 20 percent) to reduce power consumption and for better peak detection. So a fixed I_d is not feasible.

Somehow, a dual loop system is required, one loop for pushing the pole to low frequency location, and another for self regulating the DC photocurrent rejection. The circuit in Fig. 3.10 meets this requirement. M_1 , M_2 , M_{ct1} , TIA and the EA still performs the pole lowering operation. On the other hand, current mirrors M_3 - M_4 , M_5 - M_6 and M_7 - M_8 senses the DC photocurrent generated by the PD and feedback the current to be cancelled through M_{ct1} .

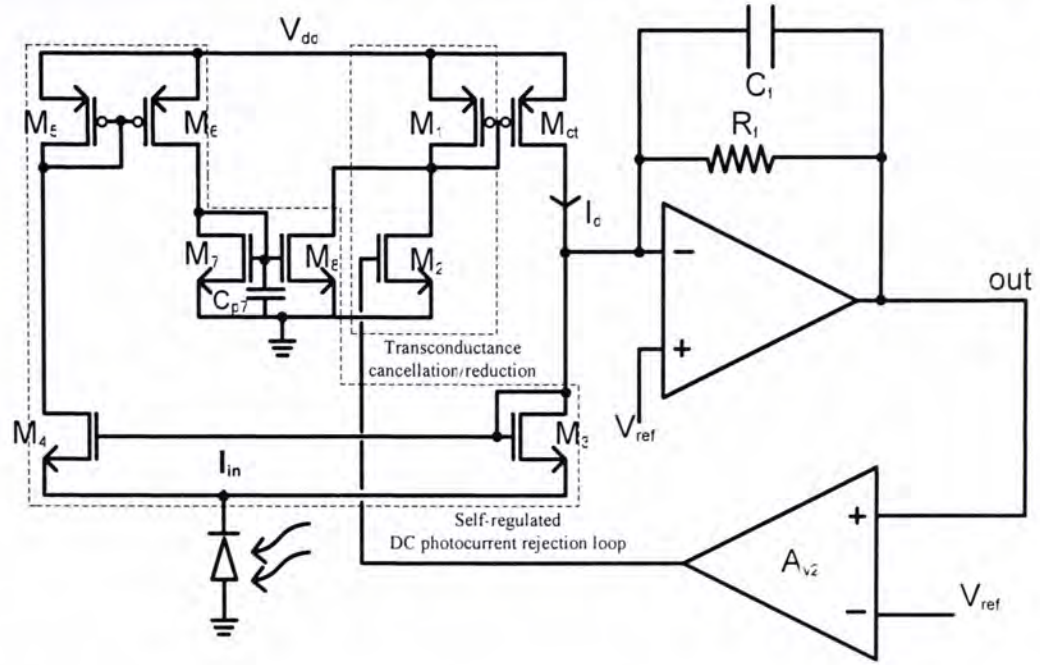


Fig. 3.10 Dual loop circuit for performing pole lowering operation and self-regulated DC photocurrent rejection.

3.2.2 Operating principle

The operation of the self-regulated DC photocurrent rejection loop goes as follows: I_{M3} has to be much greater than I_{M4} ($I_{M3} \gg I_{M4}$) in order for most DC current to be cancelled through $M3$. Concurrently, AC suppression is needed in the current rejection loop to prevent signal cancellation at I_{M3} . As a result, multiple low impedance paths are required to dissipate AC component to ground. This is achieved by squeezing very small amount of current (50 to 500-nA, thus very small g_m) through very large transistor (to generate large parasitic capacitor for filtering) – $M7$ - $M8$ and $M1$ - M_{ctl} . However, in the actual design, the second zero location generated by the self-regulated DC photocurrent rejection loop is not low enough (the first pole is generated by the pole frequency control loop going through R_f , EA and $M2$); hence, there is a 3-dB AC suppression near the vicinity of lower-band f_{-3dB} in the overall frequency response. Ideally, this pole (it is a zero looking at the output impedance of V_{o1} , pole otherwise) generated by the self-regulated rejection loop should be designed such that it aligns with the attenuation curve of the signal taken at the drain of $M2$, as shown in Fig. 3.11. With this design, though g_{mctl} is 80 times of g_{m1} to reduce power consumption, using $C_m = 165$ -pF, and g_{m2} of 757.5-nA/V ($W/L = 0.5/90$), and $C_{p7} = 7.19$ -pF ($W/L = 320/120$) to push the zero location to low enough frequency, an effective capacitance of 705-pF is implemented to push the pole to low

frequency location (300-Hz). A factor of 8 times reduction in capacitor size. Thus, transistor M_2 is extremely effective in compensating for the increase in (g_{mcl}/g_{m1}) and lowering the pole frequency location, as seen in Eq. 3.4.

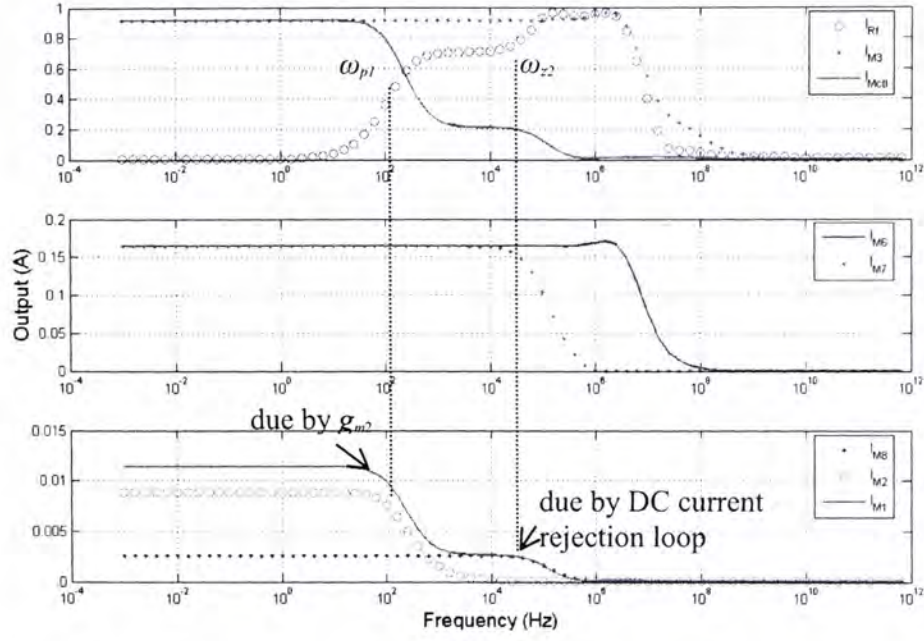


Fig. 3.11 Illustration of zero generated by the self-regulated rejection loop (the pole in I_{M1} , bottom) results in 3dB drop near the vicinity of the lower-band f_{-3dB} in I_{Rf} (top).

3.2.3 Development of the analytic model

Below (Fig. 3.12) is the small signal diagram of the dual-loop TIA.

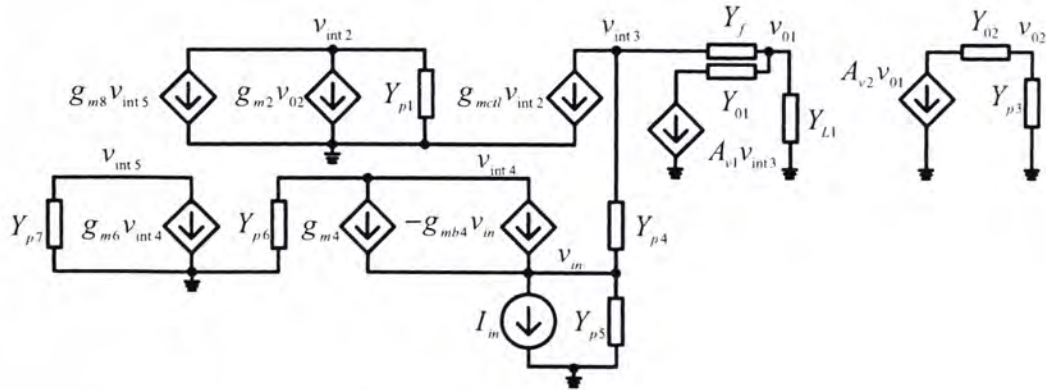


Fig. 3.12 Small signal diagram of the circuit in Fig. 3.10.

Here are the parasitic components:

$$Y_{p1} = SC_{p1} + g_{m1} \Rightarrow C_{p1} = C_{gs1} + C_{dg8} + C_{dg2} + C_{gsmcl} \quad (3.5)$$

$$Y_{p3} = SC_{p3} \Rightarrow C_{p3} = C_{gs2} + C_m \quad (3.6)$$

$$Y_{p4} = SC_{p4} + (g_{m3} + g_{mb3}) \Rightarrow C_{p4} = C_{gs3} + C_{gs4} + C_{dgmidl} \quad (3.7)$$

$$Y_{p5} = SC_{diode} \quad (3.8)$$

$$Y_{p6} = SC_{p6} + g_{m5} \Rightarrow C_{p6} = C_{gs5} + C_{gs6} + C_{dg4} \quad (3.9)$$

$$Y_{p7} = SC_{p7} + g_{m7} \Rightarrow C_{p7} = C_{gs7} + C_{gs8} + C_{dg6} \quad (3.10)$$

$$Y_{01} = 1/R_{01} \quad (3.11)$$

$$Y_{02} = 1/R_{02} \quad (3.12)$$

$$Y_f = SC_f + 1/R_f \quad (3.13)$$

$$Y_{L1} = S(C_{outA1} + C_{INA2} + C_L) \quad (3.14)$$

Now, with all the parasitic information included, we are ready to proceed with the SFG analysis. Since the theory of SFG has already been addressed extensively elsewhere [13]-[14], [29], readers are encouraged to consult these for further information. The SFG with feedback is superimposed on the circuit schematic in Fig. 3.13. From it, we see that SFG helps with the visualization of signal flow and dynamic behavior within the circuit. To help with simplification, the SFG is redrawn in Fig. 3.14 and 3.15 to highlight the feedback loops in the circuit. The circuit contains four feedback loops: L_1 , the transconductance feedback that is associated with the common-gate configuration of M_3 and M_4 , L_2 , the feedback loop that extends from the input terminal (source of M_3) through the self-regulating DC photocurrent rejection loop, which includes current mirror M_3 - M_4 , M_5 - M_6 and M_7 - M_8 , M_1 - M_{ctl} and the feedback elements in the TIA, L_3 , the self loop that is very similar to L_2 but excluding the input terminal, and L_4 , which is the feedback loop that extends from the negative input terminal of the TIA to the EA, M_2 , M_1 - M_{ctl} , namely, the loop that enables the low frequency pole. The presence of multiple loops makes this structure difficult for analysis using conventional feedback techniques.

The transimpedance gain of the circuit with feedback loop can be determined using Mason's direct rule. The basic expression is

$$\frac{V_{out}}{I_{in}}(s) = \frac{P_1 \Delta_1}{1 - (L_1 + L_2 + L_3 + L_4) + (L_1 L_4 + L_1 L_3)} \quad (3.15)$$

where P_1 is the forward transmission path from I_{in} to V_{out} ,

$$P_1 = \frac{[Y_{p1}Y_{p6}Y_{p7}Y_{p4} - (g_{m4} + g_{mb4})g_{m6}g_{m8}g_{mctl}](Y_f + A_{v1}Y_{01})}{(Y_{p4} + Y_{p5})Y_{p1}Y_{p6}Y_{p7}(Y_f + Y_{01} + Y_{L1})(Y_f + Y_{p4})} \quad (3.16)$$

and loops L_1, L_2, L_3 and L_4 are given by

$$L_1 = \frac{-(g_{m4} + g_{mb4})}{(Y_{p4} + Y_{p5})} \quad (3.17)$$

$$L_2 = \frac{[Y_{p1}Y_{p6}Y_{p7}Y_{p4} - (g_{m4} + g_{mb4})g_{m6}g_{m8}g_{mctl}](Y_{p4} + g_{m4})}{(Y_{p4} + Y_{p5})Y_{p1}Y_{p6}Y_{p7}(Y_{p4} + Y_f)} \quad (3.18)$$

$$L_3 = \frac{g_{m4}g_{m6}g_{m8}g_{mctl}}{Y_{p1}Y_{p6}Y_{p7}(Y_f + Y_{p4})} \quad (3.19)$$

$$L_4 = \frac{[(Y_{02} + Y_{p3})Y_{p1}Y_f + g_{m2}g_{mctl}A_{v2}Y_{02}](Y_f + A_{v1}Y_{01})}{(Y_{02} + Y_{p3})Y_{p1}(Y_f + Y_{01} + Y_{L1})(Y_f + Y_{p4})} \quad (3.20)$$

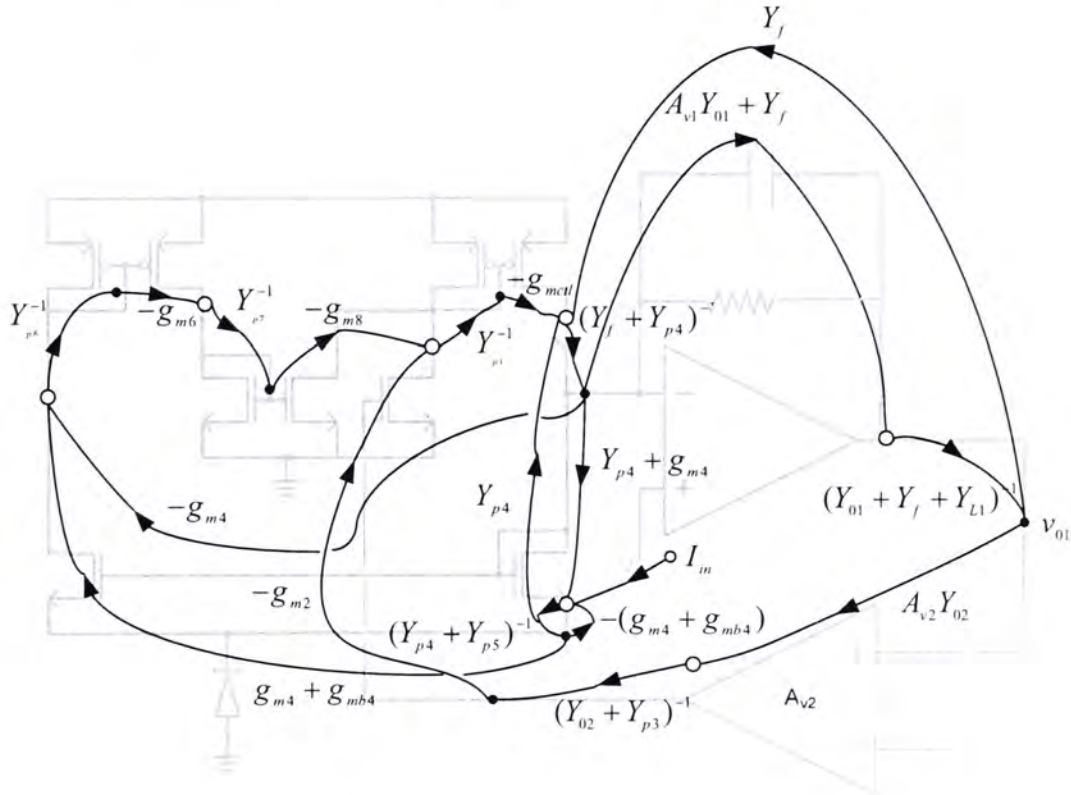


Fig. 3.13 SFG with feedback is superimposed on the circuit schematic.

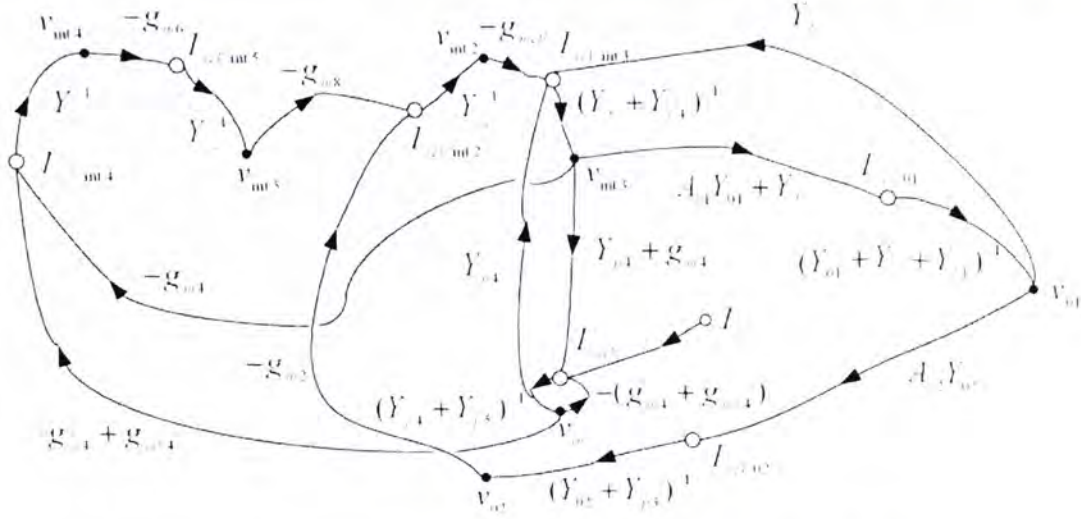


Fig. 3.14 Redrawing of the SFG in Fig. 3.13.

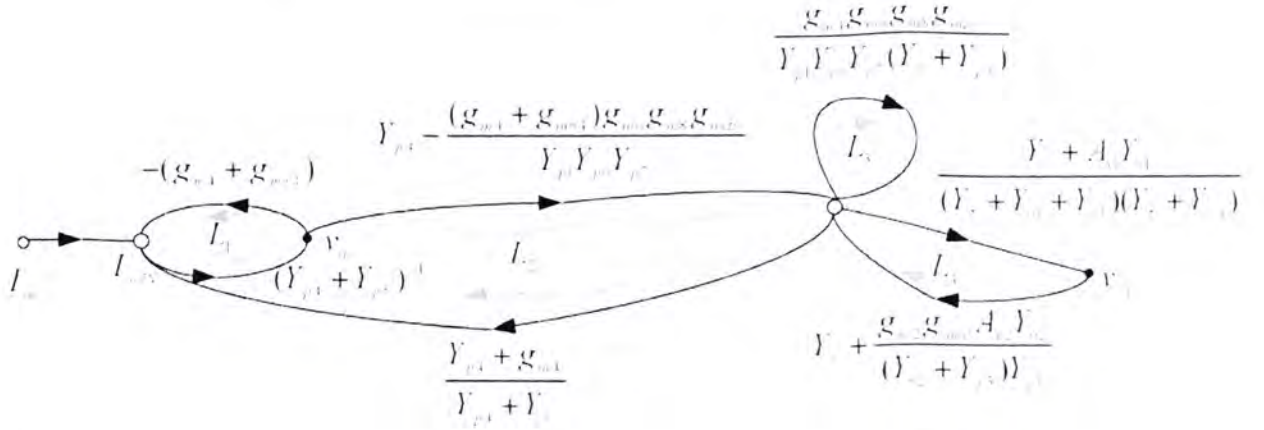


Fig. 3.15 Simplification of the SFG in Fig. 3.14 to highlight the feedback loops in circuit.

By combining Eqs. 3.5 through 3.20, the following expression is obtained for the transimpedance gain:

$$\frac{V_{out}}{I_{in}}(s) = \frac{b_2 s^2 + b_1 s + b_0}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (3.21)$$

where the coefficients are given by (details in Appendix A and CD-ROM)

$$b_2 = 0.5 \cdot C_m R_{02} \left(\frac{1}{R_f} + g_{m3t} \right) g_{m3t} [C_{p1} (g_{m3t} g_{157} - g_{4T68CTL}) g_{157} + g_{m1} (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5}) (2g_{m3t} g_{157} - g_{4T68CTL})]$$

$$b_1 = 0.5 \cdot C_m R_{02} \left(\frac{1}{R_f} + g_{m3t} \right) g_{m1} g_{157} g_{m3t} (g_{m3t} g_{157} - g_{4T68CTL})$$

$$b_0 = 0.5 \cdot g_{m1} g_{157} g_{m3t} \left(\frac{1}{R_f} + g_{m3t} \right) (g_{m3t} g_{157} - g_{4T68CTL})$$

$$\begin{aligned}
 a_3 &= \left(\frac{g_{m3t}}{R_f}\right)^2 C_m R_{02} \{g_{157} (2C_{p1} C_{p7} g_{m1} g_{m5} + g_{m7} C_{p1}^2 g_{m5}) + (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5}) \\
 &\quad (2C_{p1} g_{157} + C_{m7} g_{p1}^2 g_{m5} + C_{p1} g_{4T68CTL} R_f) + g_{m1} (g_{157} + g_{4T68CTL} R_f) [C_{p7} C_{m1} g_{m5} + ((C_f + C_L) R_f \\
 &\quad + \frac{(C_f + C_{p4}) R_f}{1 + g_{m3t} R_f}) (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5})]\} \\
 a_2 &= \left(\frac{g_{m3t}}{R_f}\right)^2 C_m R_{02} [g_{157} (2C_{p1} g_{157} + C_{p1} g_{4T68CTL} R_f + C_{p7} g_{p1}^2 g_{m5}) + g_{m1} (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5}) \\
 &\quad (g_{157} + g_{4T68CTL} R_f)] \\
 a_1 &= \left(\frac{g_{m3t}}{R_f}\right)^2 (g_{157} + g_{4T68CTL} R_f) g_{157} C_m g_{m1} R_{02} \\
 a_0 &= \left(\frac{g_{m3t}}{R_f}\right)^2 (g_{157} + g_{4T68CTL} R_f) g_{157} g_{mcl} g_{m2} R_f A_{v2}
 \end{aligned}$$

where $g_{157} = g_{m1} g_{m5} g_{m7}$, $g_{m3t} = g_{m3} + g_{mb3}$, $g_{4T68CTL} = g_{m4t} g_{m6} g_{m8} g_{mcl}$, and $g_{m4t} = g_{m4} + g_{mb4}$.

At DC, the transimpedance gain is

$$\frac{V_{out}}{I_{in}}(0) = \frac{b_0}{a_0} = \frac{g_{m1} R_f \left(\frac{1}{R_f} + g_{m3t}\right) (g_{m3t} g_{157} - g_{4T68CTL})}{g_{m2} g_{m3t} g_{mcl} A_{v2} (g_{157} + g_{4T68CTL} R_f)} \quad (3.22)$$

To verify the accuracy of Eq. 3.21, four designs with different sets of transistor and opamp parameters were used. These circuits were simulated in SPICE and then small-signal parameters were extracted and substituted in Eq. 3.21. The analytic and SPICE simulation results are plotted together in Fig. 3.16. The results are in excellent agreement within 1-dB and validate the initial approximations made in the small-signal circuit. Nevertheless, the simulated results deviate from the ideal case and Eq. 3.4, in that the lower-band f_{-3dB} should remain independent of the input DC photocurrent. Actually, f_{-3dB} varies from 32.6-Hz to 251-Hz, and g_{m2} varies from 106.3-nA/V to 838.5-nA/V for different amounts of I_{dc} in simulation. Possibly, the error voltage integrated by the EA is slightly different for each and is proportional to I_{dc} due to differences in DC level of V_{01} ; hence, a range of control voltages are generated for different I_{dc} , which result in different g_{m2} . Fortunately, a tuning mechanism for the lower-band f_{-3dB} is established by means of varying the amount of DC current through the natural behavior of the circuit. Since Eq. 3.21 is large and cumbersome for design purpose, a simplified set of equations are required for design and optimization. The following section is devoted to model and noise derivation.

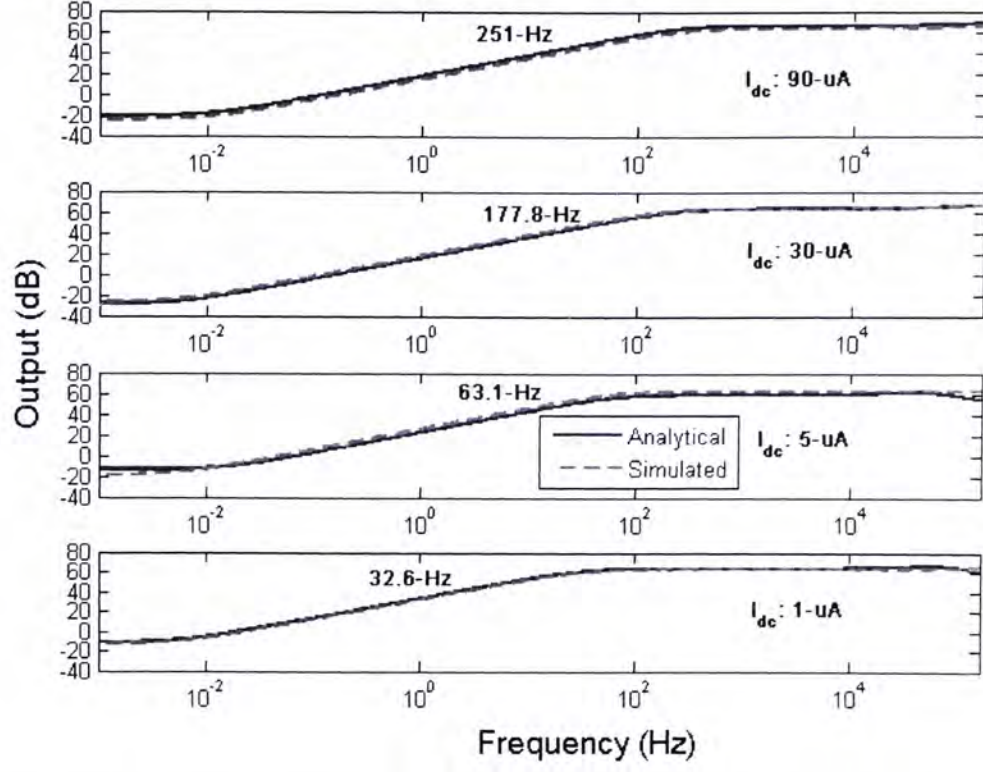


Fig. 3.16 The plot of system transfer function from analytical simulation vs. SPICE simulation result for comparison, for different levels of DC currents.

3.2.4 Derivation of frequency response

The first zero can be obtained by the following (see Eq. 3.21); assuming that $b_2 \ll b_1$:

$$\omega_{z1} \cong \frac{b_0}{b_1} = \frac{g_{m1} g_{157} g_{m3t} \frac{A_{v1}}{R_{01}} \left(\frac{1}{R_f} + g_{m3t} \right)^2 (g_{m3t} g_{157} - g_{4T68CTL})}{C_m R_{02} \left(\frac{1}{R_f} + g_{m3t} \right)^2 g_{m1} g_{157} g_{m3t} \frac{A_{v1}}{R_{01}} (g_{m3t} g_{157} - g_{4T68CTL})} = \frac{1}{R_{02} C_m} \quad (3.23)$$

To calculate the first lower-band f_{-3dB} , we compute the output impedance at V_{02} by using the SFG of Fig. 3.2, which is shown below in Fig. 3.17:

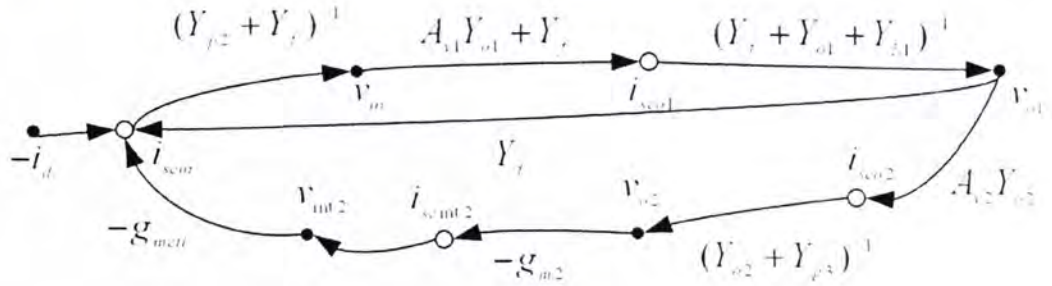


Fig. 3.17 SFG of Fig. 3.9.

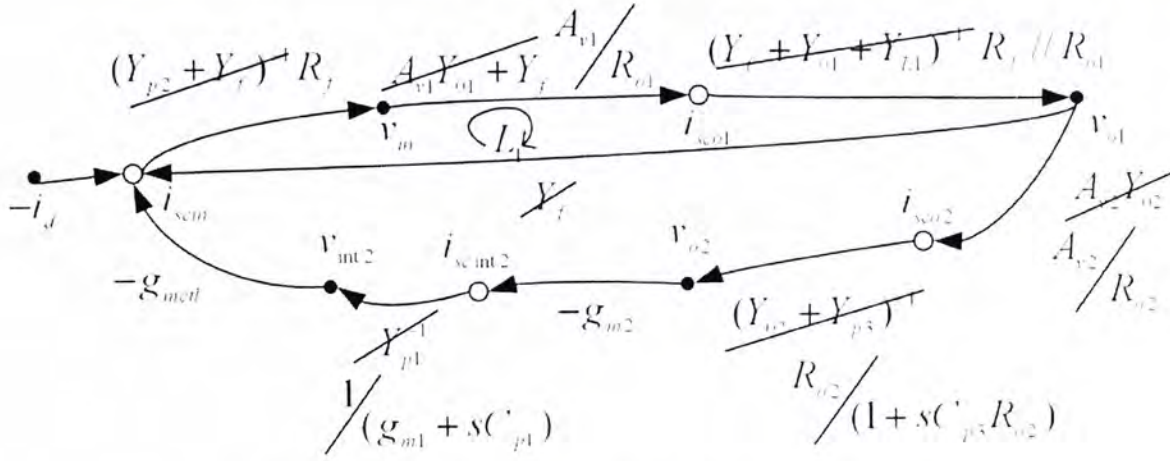


Fig. 3.18 Simplified SFG from Fig. 3.17.

Assuming $R_{o1} \gg R_f$, we have on the upper path of L_1 , $R_f^2 A_{v1} / R_{o1}$, which gives

$$L_1 = \frac{R_f^2 A_{v1}}{R_{o1}} // R_f = \frac{R_f^2 A_{v1}}{R_f A_{v1} + R_{o1}}$$

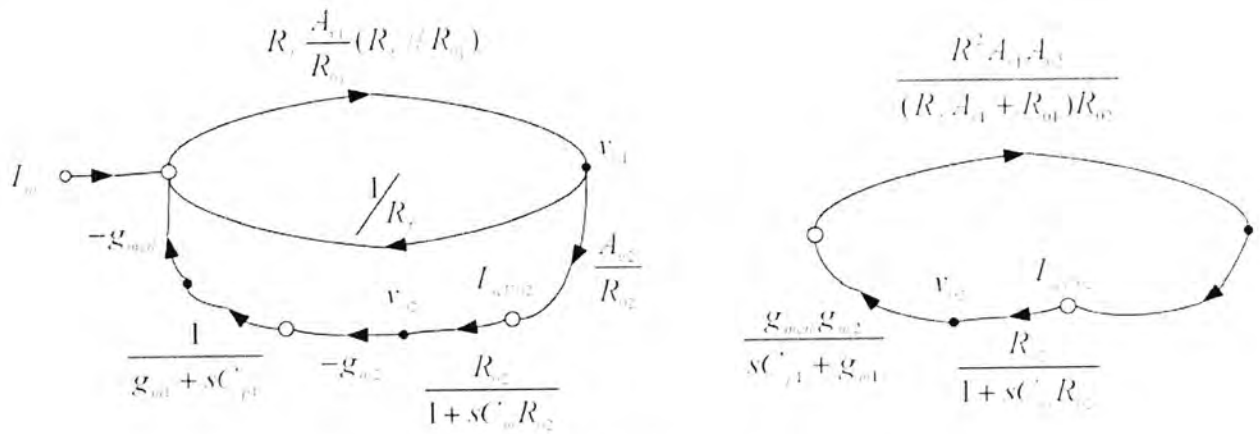


Fig. 3.19 Simplified SFG from Fig. 3.18.

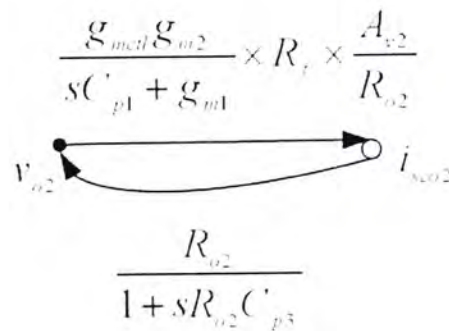


Fig. 3.20 Simplified SFG from Fig. 3.19.

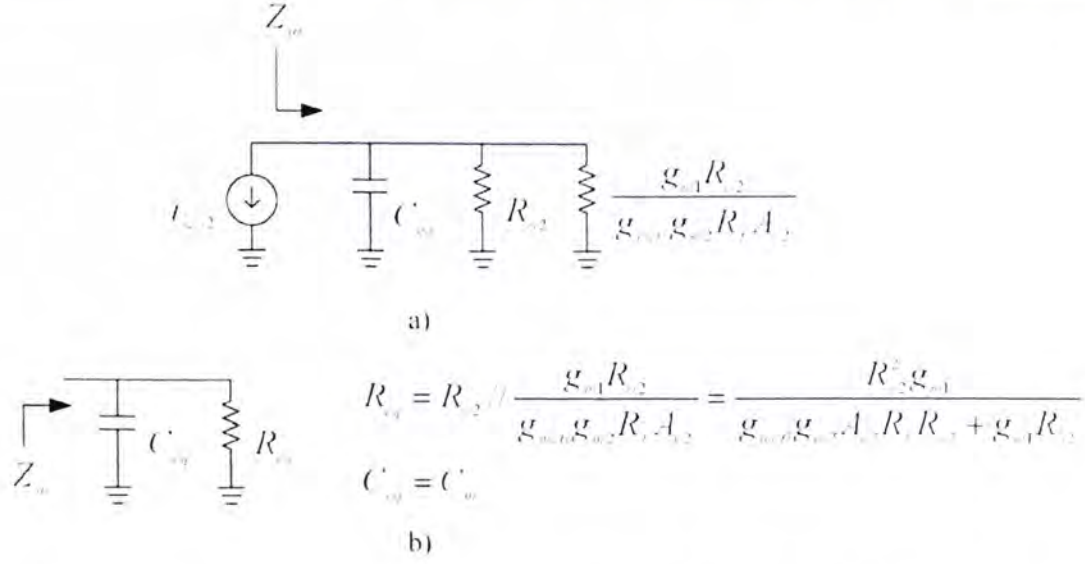


Fig. 3.21 Schematic representation of the SFG in Fig. 3.20 a) complete, b) lumped model.

From the lumped model in Fig. 3.21, the equivalent RC can be found:

$$\omega_{p1} = \frac{1}{R_{eq} C_{eq}} = \frac{1}{C_m \frac{R_{02}^2 g_{m1}}{g_{m1}g_{m2}R_fA_{v2}R_{02} + g_{m1}R_{02}}} = \frac{R_f A_{v2} g_{m1} \frac{g_{m2}}{g_{m1}}}{R_{02} C_m} \quad (3.24)$$

From ω_{p1} and ω_{z1} , we can see that the first set of pole and zero tracks each other by R_{02} and C_m and they differ by a factor of $R_f A_{v2} g_{m1} (g_{m2} / g_{m1})$. This ensures constant DC attenuation and compensates for process variation.

The second zero can be found by knowing the numerator and the first zero:

$$N(s) = b_0 \left(\frac{b_2}{b_0} s^2 + \frac{b_1}{b_0} s + 1 \right) = b_0 \left(1 + \frac{s}{\omega_{z1}} \right) \left(1 + \frac{s}{\omega_{z2}} \right) = b_0 \left[1 + s \left(\frac{1}{\omega_{z1}} + \frac{1}{\omega_{z2}} \right) + \frac{s^2}{\omega_{z1} \omega_{z2}} \right]$$

$$\frac{b_2}{b_0} = \frac{1}{\omega_{z1} \omega_{z2}}, \text{ and } \omega_{z1} = \frac{1}{R_{02} C_m}$$

$$\omega_{z2} = R_{02} C_m \frac{b_0}{b_2} = \frac{g_{m1} g_{157} (g_{m31} g_{157} - g_{4768CTL})}{C_{p1} g_{157} (g_{m31} g_{157} - g_{4768CTL}) + g_{m1} (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5}) (2g_{m31} g_{157} - g_{4768CTL})} \quad (3.25)$$

From ω_{z2} , C_{p1} , g_{m7} , C_{p1} , g_{m5} and C_{p7} , g_{m1} , g_{m5} should be designed as large as possible to align the second zero with the roll-off of frequency response in Fig. 3.11 and minimize AC suppression near the vicinity of the lower-band f_{-3dB} . The factor $g_{m31} g_{157} - g_{4768CTL}$ has repeatedly appeared and optimization based on it can be performed.

Since the denominator is a third order polynomial, there exists a complex pole:

$$D(s) = a_3 \left(s^3 + \frac{a_2}{a_3} s^2 + \frac{a_1}{a_3} s + \frac{a_0}{a_3} \right) = a_3 (s + \omega_{p1}) \left(s^2 + \frac{\omega_o}{Q} s + \omega_o^2 \right)$$

$$\omega_{p1} \omega_o^2 = \frac{a_0}{a_3}, \text{ and } \omega_{p1} = \frac{R_f A_{v2} G_{m2} \frac{G_{mctl}}{G_{m1}}}{R_{o2} C_m}$$

$$\omega_o^2 = \frac{a_0}{\omega_{p1} a_3} = \frac{g_{m1} g_{157} (g_{157} + g_{4768CTL} R_f)}{g_{157} (2C_{p1} C_{p7} g_{m1} g_{m5} + g_{m7} C_{p1}^2 g_{m5}) + (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5}) (2C_{p1} g_{157} + C_{p7} g_{m1}^2 g_{m5} + C_{p1} g_{4768CTL} R_f)} + g_{m1} (g_{157} + g_{4768CTL} R_f) [C_{p7} C_{p1} g_{m5} + ((C_f + C_L) R_f + \frac{(C_f + C_{p4}) R_f}{1 + g_{m3t} R_f}) (g_{m7} C_{p1} g_{m5} + C_{p7} g_{m1} g_{m5})] \quad (3.26)$$

After some manipulation (details to be found in Appendix B), Q is found to be

$$Q = \frac{a_1 \omega_o - a_2 \omega_o \omega_{p1}}{a_2 \omega_o^2 - a_1 \omega_{p1}}$$

Therefore, to keep Q factor small, it is preferable to push ω_o very far away from frequency of interest (increase ω_o) and make ω_{p1} smaller. This is achieved by reducing C_{p1} , C_{p4} , C_f and C_{p7} .

3.2.5 Noise derivation

The schematic in Fig. 3.22 presents the dual-loop TIA, together with its noise source:

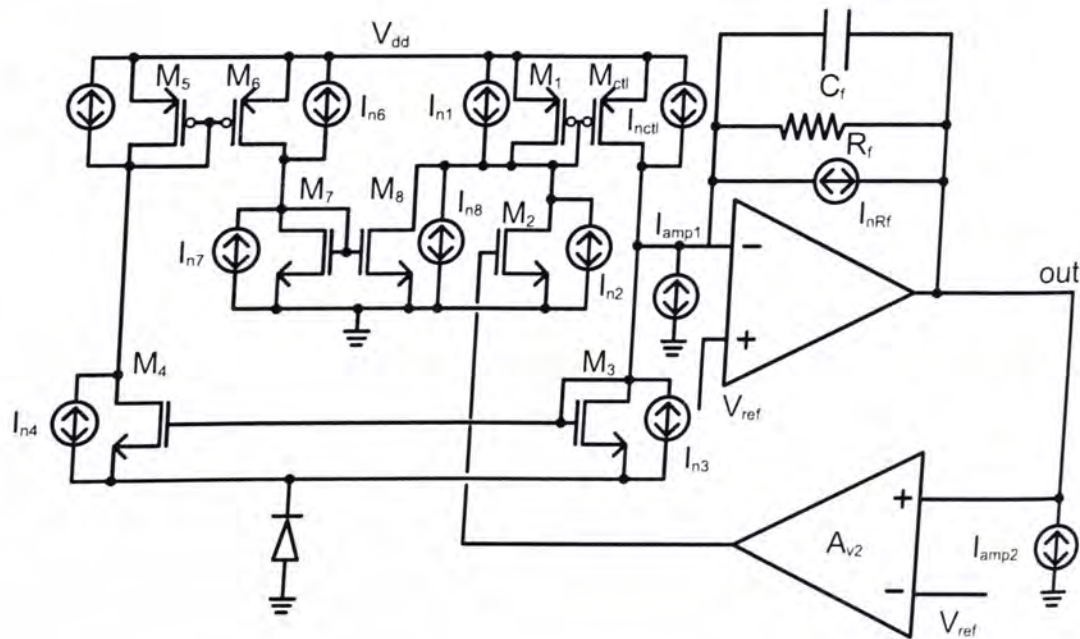


Fig. 3.22 Dual-loop transimpedance amplifier with noise sources.

Noise transfer function is derived from the SFG in Fig. 3.23 to arrive at the analytical noise model. Partial derivation of the noise transfer function for each source is attached in Appendix C in this thesis and in CD-ROM.

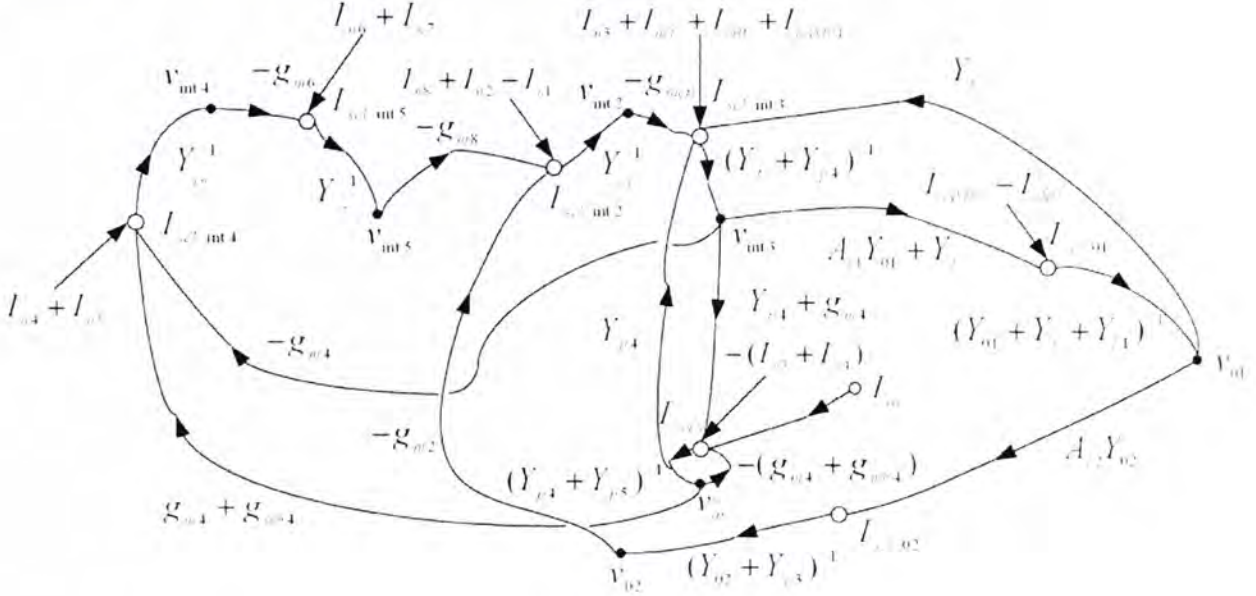


Fig. 3.23 SFG of dual-loop transimpedance amplifier with noise sources

From I_{n3} , I_{nctl} , and I_{nAMP1} :

$$I_{n3_in}^2 + I_{nctl_in}^2 + I_{nAMP1_in}^2 = \left| \frac{sA_{v1}R_{02}C_m g_{m1} + g_{m2}A_{v1}A_{v2}g_{mctl}R_f}{sb_{x1}C_m g_{m1}R_{02}R_{01}(1/R_f + g_{m3t})} \right|^2 (I_{n3}^2 + I_{nctl}^2 + I_{nAMP1}^2) \quad (3.27)$$

Since the contribution from the current sources I_{n3} , I_{nctl} and I_{nAMP1} are identical, they can be analyzed together. This equation tells us that at DC, the noise contribution from these sources are infinite. Transistors M_3 and M_{ctl} contribute most of the $1/f$ noise. For that reason, to minimize the $1/f$ noise, $g_{4768CTL}$ in b_{x1} , g_{m1} , and C_m should be increased and g_{m2} should be decreased.

From I_{n4} and I_{n5}

$$I_{n4_in}^2 + I_{n5_in}^2 = \left| \frac{sg_{m1}g_{m3t}R_{02}C_m + g_{mctl}g_{m3t}g_{m2}A_{v2}R_f}{sg_{m1}g_{m4t}R_{02}C_m + g_{mctl}g_{m4t}g_{m2}A_{v2}R_f} \right|^2 (I_{n4}^2 + I_{n5}^2) \quad (3.28)$$

Essentially, this equation tells us the noise contribution of I_{n4} and I_{n5} are negligible at low frequencies (except for the noise source itself) and is constant (g_{m3t} / g_{m4t}) throughout most of the passband because the numerator and denominator cancels with each other, so the net increase in noise is zero.

From I_{n6} and I_{n7}

$$I_{n6_in}^2 + I_{n7_in}^2 = \left| \frac{g_{m3t} g_{m5}}{g_{m4t} g_{m6}} \right|^2 (I_{n6}^2 + I_{n7}^2) \quad (3.29)$$

Identical to I_{n4} and I_{n5} , the noise contributions of I_{n6} and I_{n7} are constant throughout the passband and are minimal at low frequency.

From I_{n1} , I_{n2} and I_{n8}

$$I_{n8_in}^2 + I_{n2_in}^2 + I_{n1_in}^2 = \left| \frac{s g_{m3t} g_{m5} g_{m7} g_{m1} R_{02} C_m + g_{m3t} g_{m5} g_{m7} g_{m2} g_{mctl} A_{v2} R_f}{s g_{4T68} g_{m1} R_{02} C_m + g_{4T68} g_{m2} g_{mctl} A_{v2} R_f} \right|^2 (I_{n1}^2 + I_{n2}^2 + I_{n8}^2) \quad (3.30)$$

Again, similar to the previous analysis (I_{n4} and I_{n5}), the noise contributions of I_{n1} , I_{n2} and I_{n8} are negligible as well and are constant ($g_{m3t} g_{m5} g_{m7} / g_{m4T68}$) throughout the passband.

From I_{nRf}

$$I_{nRf_in}^2 = \left| \frac{s A_{v1} R_{02} C_m g_{m1} + g_{m2} g_{mctl} A_{v1} A_{v2} R_f}{s b_{x1} C_m g_{m1} R_{01} R_{02} \left(\frac{1}{R_f} + g_{m3t} \right)} \right|^2 I_{nRf}^2 \quad (3.31)$$

Similar to the previous analysis (I_{n3}), the noise contribution from I_{nRf} is infinite, and together with transistors M_3 and M_{ctl} , contribute most of the 1/f noise within the system. Therefore, to minimize the 1/f and low frequency noise, $g_{4T68CTL}$ in b_{x1} , g_{m1} , and C_m should be increased and g_{m2} should be decreased.

From I_{nAMP2}

$$I_{nAMP2_in}^2 = \left| \frac{s R_{02} C_m g_{m1} + g_{m2} g_{mctl} A_{v2} R_f}{s b_{x5} C_m g_{m1} R_{02} \left(\frac{1}{R_f} + g_{m3t} \right)} \right|^2 I_{nAMP2}^2 \quad (3.32)$$

The noise transfer function from I_{nAMP2} to I_{nAMP2_in} resembles the previous analysis (I_{n3}), in that the noise contribution from I_{nAMP2} is infinite, and together with transistors M_3 and M_{ctl} , contribute significant amount of 1/f noise. Accordingly, to minimize the 1/f noise, $g_{4T68CTL}$ in b_{x5} , g_{157} , and C_m should be increased and g_{m2} should be decreased.

Total input referred noise

The total input referred noise of the dual-loop TIA is given by the sum of the individual contribution from each component (Eqs. 3.27 through 3.32):

$$I_{ni_total}^2 = I_{n8_in}^2 + I_{n2_in}^2 + I_{n1_in}^2 + I_{n3_in}^2 + I_{nctl_in}^2 + I_{nAMP1_in}^2 + I_{n4_in}^2 + I_{n5_in}^2 + I_{n6_in}^2 + I_{n7_in}^2 + I_{nRf_in}^2 + I_{nAMP2_in}^2$$

where

$$b_{x1} = \frac{1 - \frac{g_{4T68CTL}}{g_{m3t} g_{157}}}{1 - \frac{g_{m3t}}{g_{m3t} + 1/R_f} (1 - \frac{g_{4T68CTL}}{g_{m3t} g_{157}})}, \text{ and } b_{x5} = \frac{g_{m3t} g_{157} - g_{4T68CTL}}{g_{m3t} (\frac{g_{157}}{R_f} + g_{4T68CTL})}$$

$$I_{nX} = 4kT \frac{2}{3} g_{mX} + \frac{g_{mX}^2 K}{W_X L_X C_{ox} f}, \quad I_{nRf} = \frac{4kT}{R_f}, \quad K = 5.1e-27 \text{ for NMOS and } 8.5e-27 \text{ for PMOS, which are process specific, and } k = 1.38e-23.$$

In the noise calculation, both 1/f and thermal noise are included in the noise source since 1/f noise dominates in the low frequency region, which is the operating frequency of the circuit. From Fig. 3.24, M_3 , R_f and M_{ctl} contribute the most noise across a wide range of frequency while M_1 contributes a significant amount of noise in the passband at $I_{dc} = 30 \mu A$.

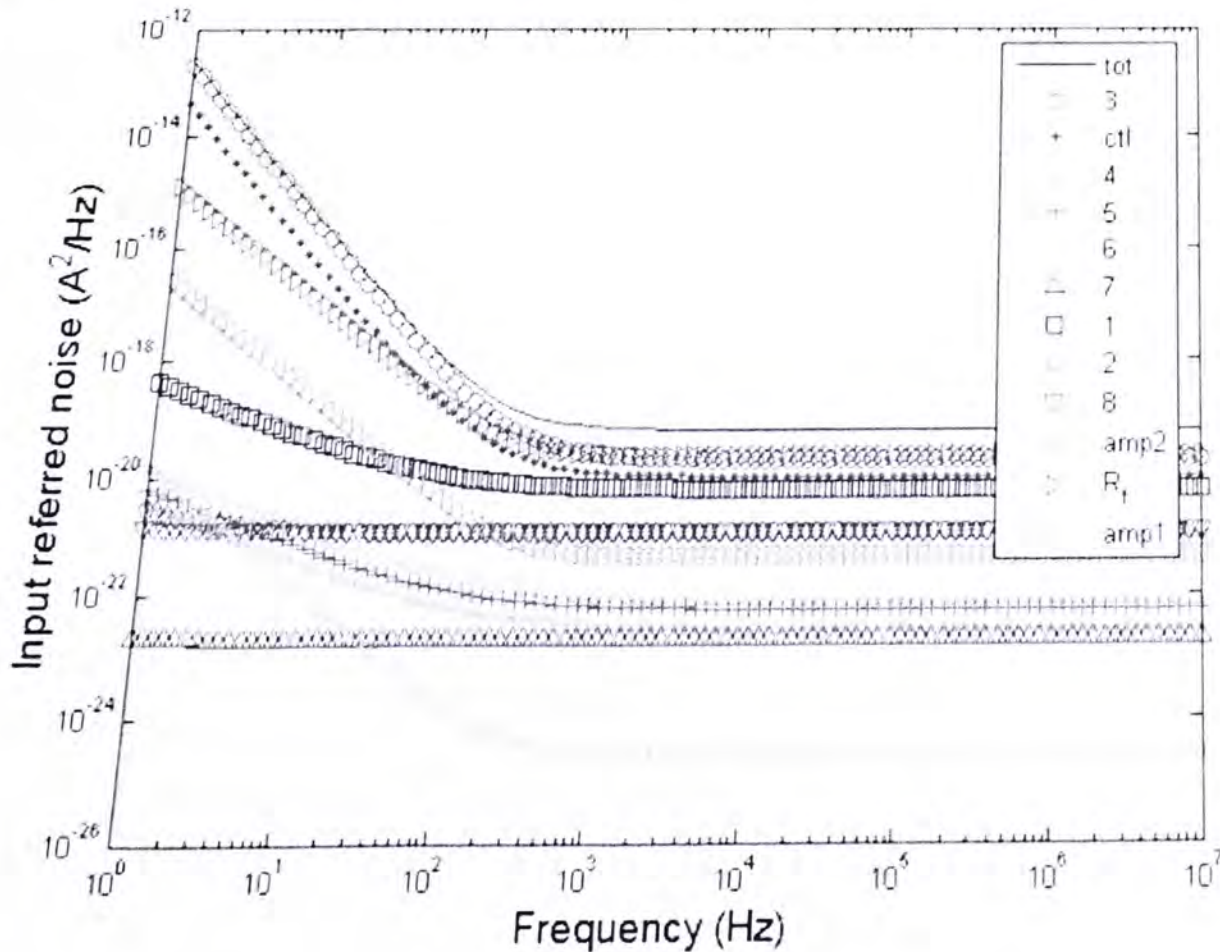


Fig. 3.24 Input referred noise of the individual transistors and opamps (at $I_{dc} = 30 \mu A$) within the dual-loop transimpedance amplifier.

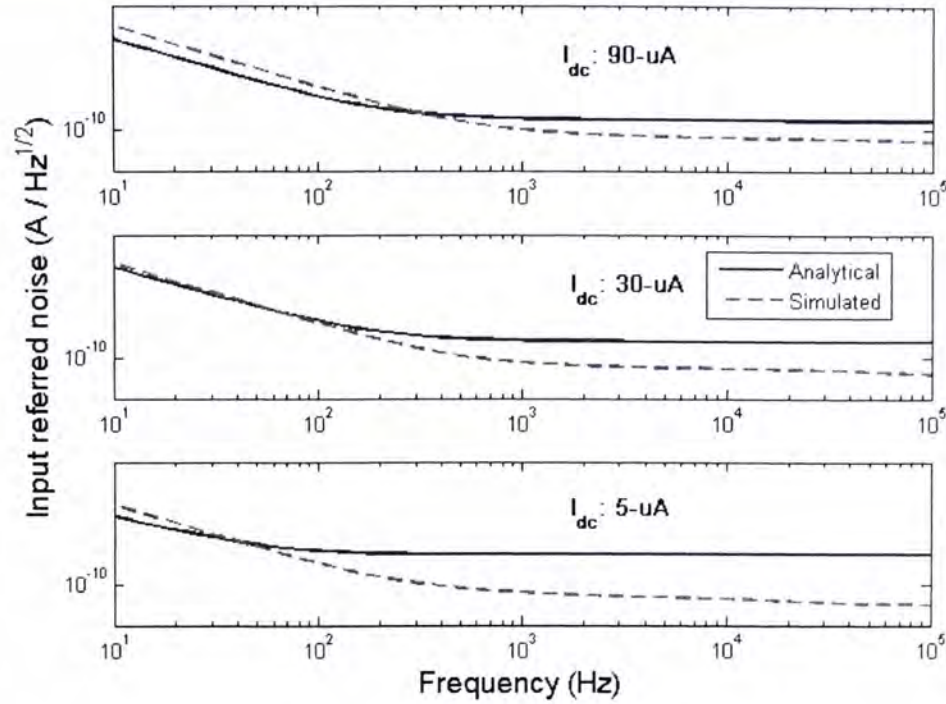


Fig. 3.25 The input referred noise from analytical simulation result and SPICE simulation result are shown together.

However, when this analytical result is compared with the actual schematic simulation in Cadence using Spectre, a discrepancy in the noise behavior is observed with the change of one of the parameter – R_f . Theoretically, according to Eqs. 3.27, 3.31 and 3.32, an increase in noise is predicted with the increase of R_f (an extra R_f in numerator); this is certainly not the case with the schematic simulation using Spectre. Possibly, a mistake is made in the derivation of the noise transfer function of M_3 , R_f and error amplifier. At the time of thesis writing, this issue still is still under investigation and hopefully a correction can be made in the near future. Nonetheless, the $1/f$ noise trend in Fig. 3.25 is predicted very accurately by the equation, however as frequency increases, the analytical result deviates from the simulation possibly due to approximation error at higher frequency. This is not an issue here since we are mostly concerned with the noise behavior of the circuit at frequency less than 5-KHz.

From Eqs. 3.23 to 3.26, and the noise equations, design optimization can be performed and deeper understanding of the system can be gained through studying this set of equations.

3.3 Implementation and experimental results

In this section, the measurement result and implementation details from the off-chip capacitor TIA and the dual-loop TIA are presented. Both circuits are implemented in AMS 0.35- μm CMOS technology and Fig. 3.26 shows overall micrograph. The measurement results of the overall system in Fig. 2.7 and the CS-LPF will be revealed in latter half of Chapter 4.

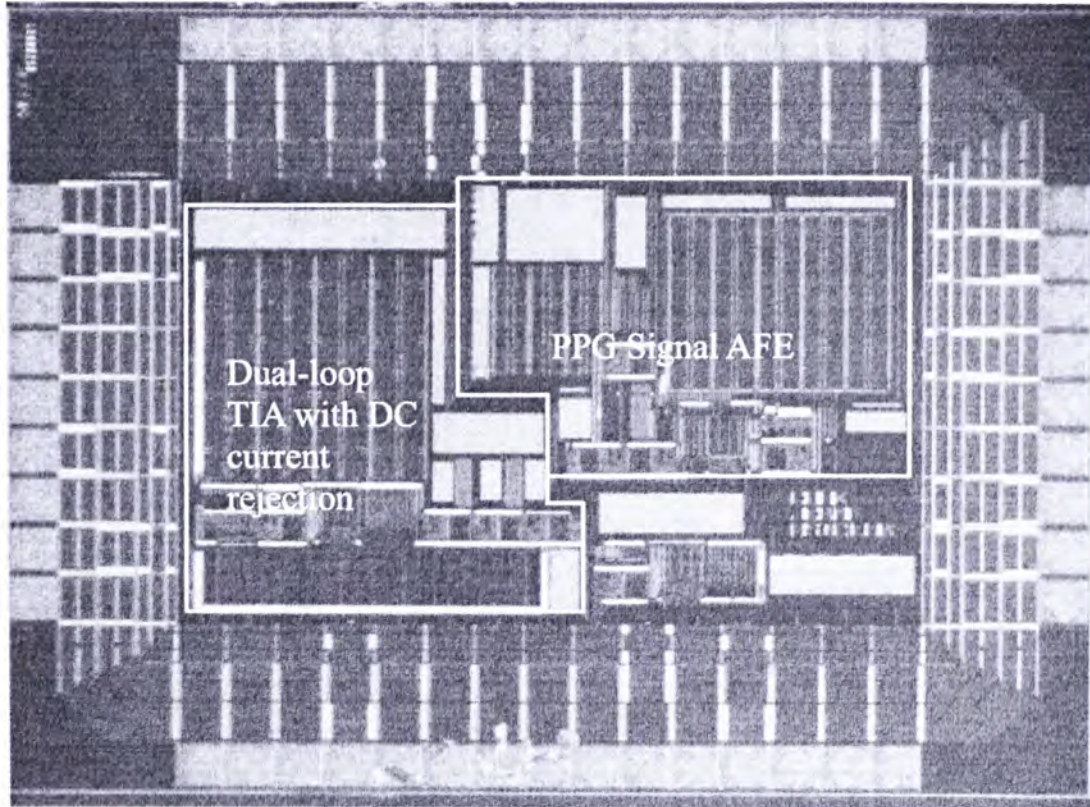


Fig. 3.26 Micrograph of entire chip.

3.3.1 Off-chip capacitor TIA

The micrograph of the off-chip capacitor TIA is shown in Fig. 3.27. The size of just the off-chip capacitor TIA is about $451\text{-}\mu\text{m} \times 600\text{-}\mu\text{m}$ and occupies an area of about 0.27-mm^2 . It operates from a 2.5-V supply and consumes about $149.6\text{-}\mu\text{W}$ of power. Extra care is taken in laying out the large C_H such that parasitic impedance from the signal path to the bottom plate of the capacitor is minimized. In addition, components are placed as close to each other as possible to minimize length of signal path. The test fixture in Fig. 3.28 consists of a DC blocking circuit with bias, opamp, transistor and resistor in the source follower configuration, which forms the current source generator and timer (74HC4538N) to generate the necessary clock

waveforms for the LED driver and the S/H. The input can be switched between the current source and the actual sensor unit (Waitrony RS-05FS). Variable amount of DC current is generated by varying the values of R_i in the fixture. In all the testing of the off-chip capacitor TIA, the LED is pulsed at 100-Hz with a 10% (900- μ s every 10-ms) duty cycle. And f_{clk} in S/H is about 100-Hz as well (700- μ s every 10-ms). The sampling pulse occurs within the onset of the LED pulse.

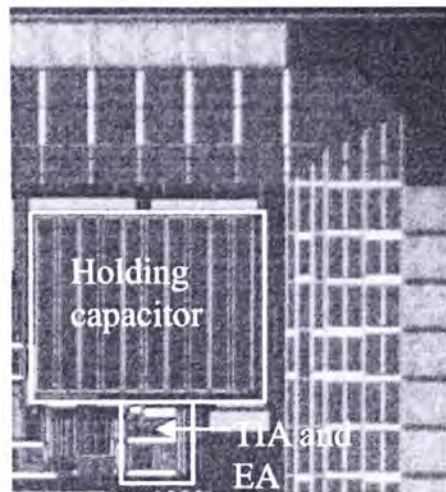


Fig. 3.27 Micrograph of off-chip capacitor TIA.

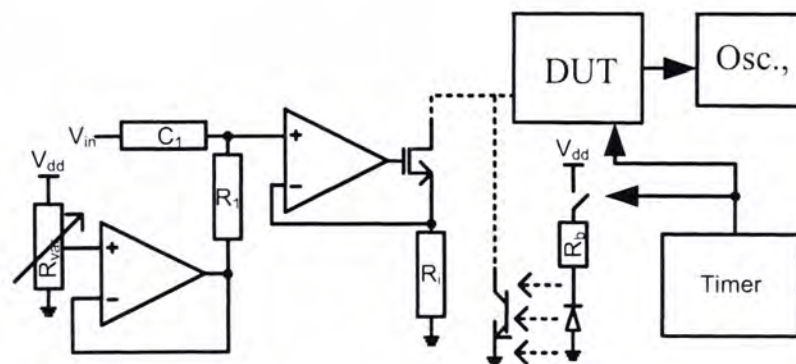


Fig. 3.28 Test fixture for the off-chip capacitor TIA.

Measurement results

Fig. 3.29 gives the output of the off-chip capacitor TIA during start-up, which is taken at the S/H when the finger is placed onto the sensor unit. A disturbance is introduced to the system as the finger is placed onto the sensor; hence the overshoot in voltage level and the feedback mechanism starts to perform regulation of DC output biasing point and set the output to the correct level. The signal settles at 1.259-V and the settling time is about 1.68-s, which is reasonable since the circuit

operates at very low frequency. The inset shows the zoom in version of the settled signal.

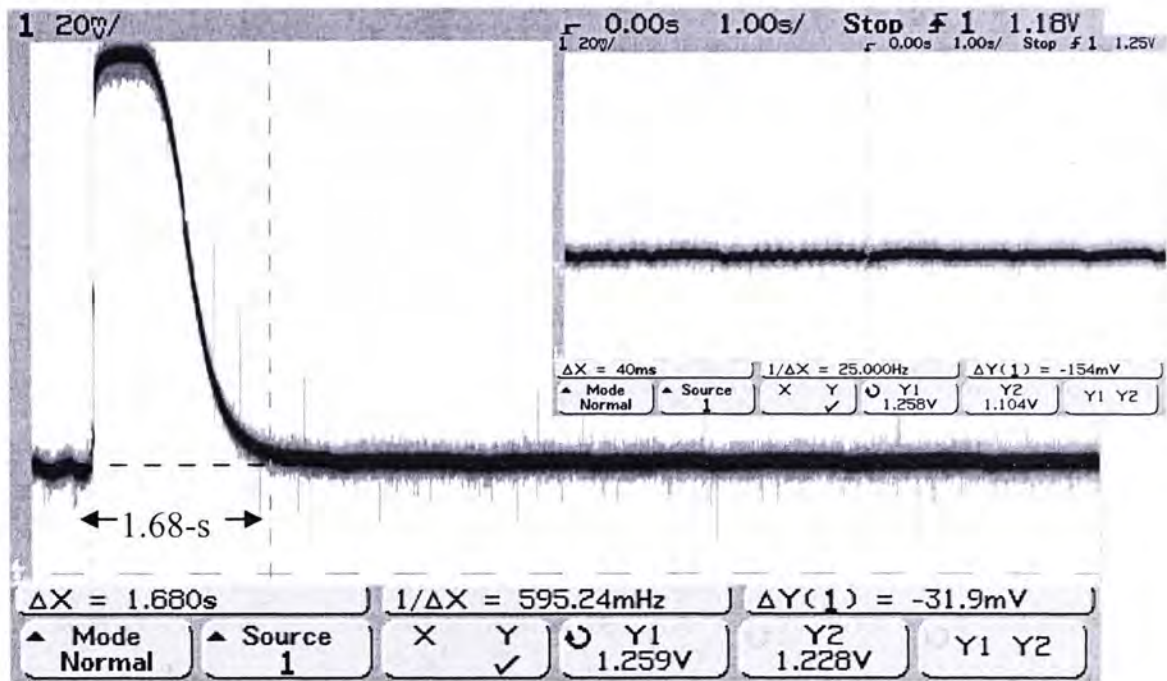


Fig. 3.29 Output of sample-and-hold circuit during start-up and the signal settles at 1.259 V. Settling time is about 1.68s.

Fig. 3.30 shows the output waveform at the off-chip capacitor TIA, together with the clock waveform. The voltage waveform in Fig. 3.30 shows charge leakage in the switches of the S/H circuit as a result of insufficient C_H . This can be relieved by using a larger C_H , proper switch size and lastly, a high order lowpass filter to eliminate the high frequency spurs. Fig. 3.31 portrays the frequency response of the off-chip capacitor TIA. Only highpass response is shown here because only the lower-band f_{-3dB} is concerned here and the upper-band f_{-3dB} at 15-MHz is not important. The highpass response is given by Eq. 3.3, which is the result of using a 240-nF off chip capacitor. There are two curves in this figure that corresponds to DC current of 5.8- μ A and 22.0- μ A, respectively. For $I_{dc} = 22 \mu$ A and 5.8 μ A, the cutoff frequency are both 0.6-Hz. And these corroborate with the simulation results in Fig. 3.5 very closely.

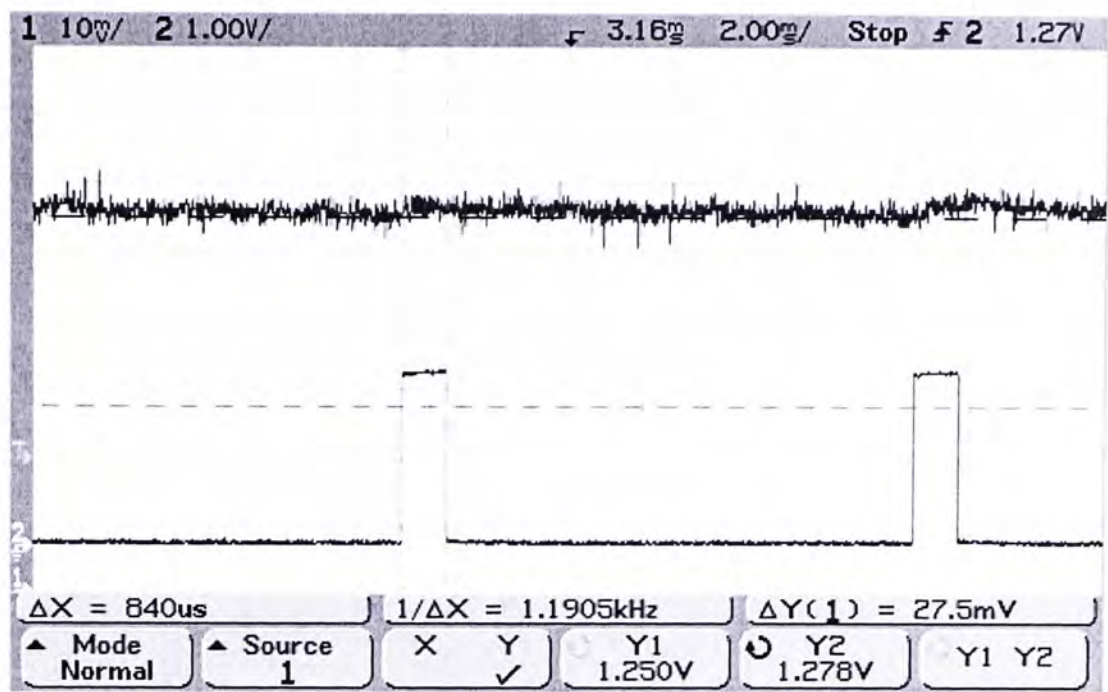


Fig. 3.30 Output waveform at the off-chip capacitor TIA, together with the clock waveform.

Fig. 3.32 illustrates the DR of the off-chip capacitor TIA. As can be seen from the figure, the DR is extremely limited and the THD is quite high. Nonetheless, not all are lost since a lowpass filter with very low cutoff frequency follows this off-chip capacitor TIA to attenuate the high frequency spurs from modulation and also the undesirable harmonics. Hence, signal integrity is preserved.

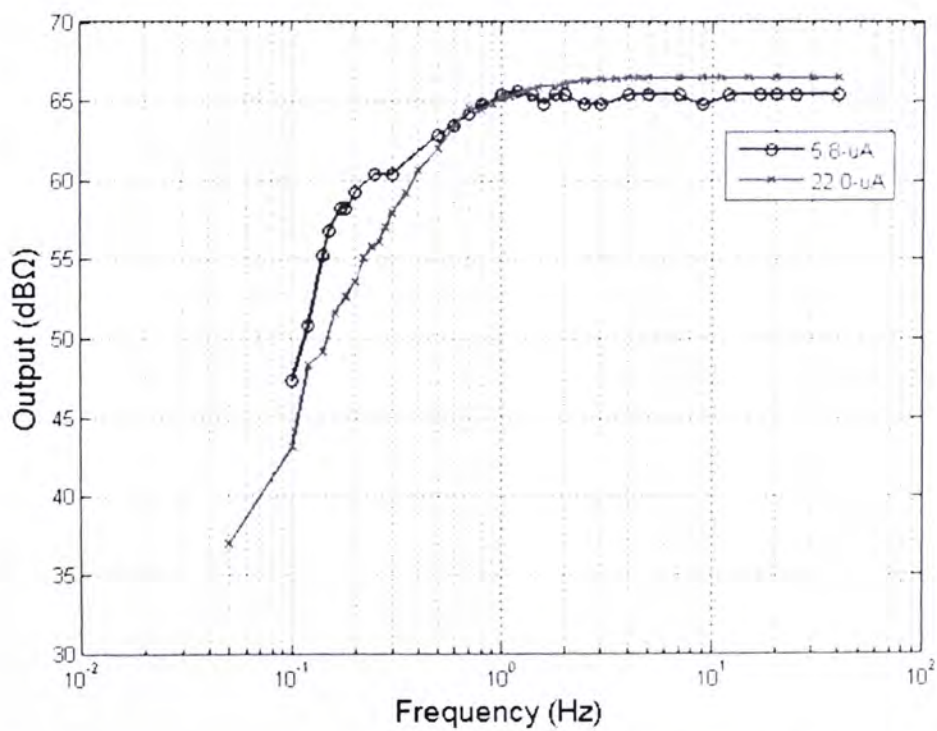


Fig. 3.31 Frequency responses of the off-chip capacitor TIA only at different I_{dc} .

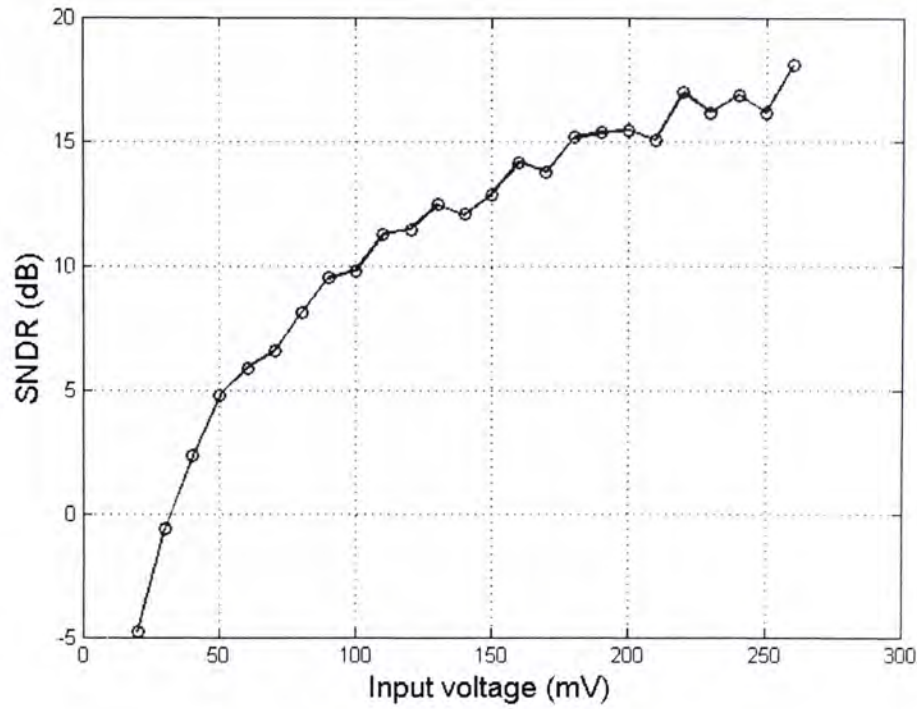


Fig. 3.32 DR of TIA only at $I_{dc} = 3 \mu\text{A}$. For a 10-dB SNDR ($\sim 17.8\%$ THD), the DR is about 13.97-dB.

3.3.2 Dual-loop TIA

The micrograph and the aspect ratios of the dual-loop TIA are shown in Fig. 3.33 and Table 3.2. The circuit is about $746\text{-}\mu\text{m}$ by $902\text{-}\mu\text{m}$, occupies an area of about 0.67-mm^2 , and consumes about $155.8\text{-}\mu\text{W}$ of power from a 2.5-V supply at $I_{dc} = 20 \mu\text{A}$. Extra care is taken in laying out transistors with very small aspect ratio (M_7 , M_8 and M_2) using common-centric and very long transistor is divided into several shorter transistors. In addition, components are placed as close to each other as possible to minimize length of signal path. The test fixture is shown in Fig. 3.34, which is very similar to the test fixture used to measure the off-chip capacitor TIA. In the following section, measurement results from $V_{dd} = 2.5\text{-V}$ is presented.

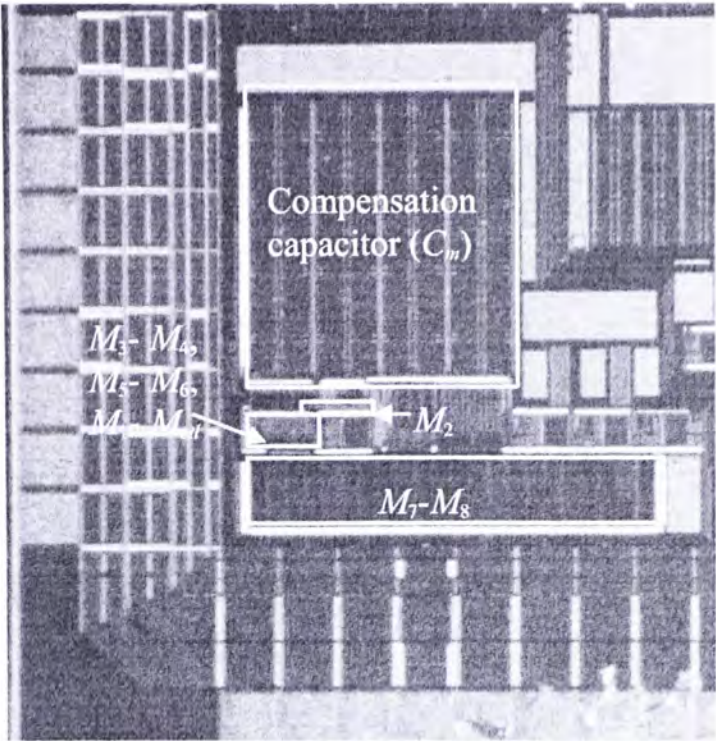


Fig. 3.33 Micrograph of the dual-loop TIA.

Loop component (refer to Fig. 3.10, all units in μm)	TIA opamp (refer to Fig. 3.3a, all units in μm)	EA opamp (refer to Fig. 3.3a, all units in μm)
$M_{c11} = 200 / 4$	$M_{1,2} = 16 / 2.8$	$M_{1,2} = 0.8 / 8.4$
$M_1 = 2.5 / 4$	$M_{3,4} = 2.75 / 1.8$	$M_{3,4} = 1.8 / 11.2$
$M_2 = 0.5 / 90$	$M_5 = 4.3 / 1.4$	$M_5 = 1.4 / 4.2$
$M_3 = 280.5 / 1.2$	$M_6 = 31 / 0.75$	$M_6 = 20 / 3.6$
$M_4 = 25.5 / 1.2$	$M_7 = 46 / 1.4$	$M_7 = 2.9 / 4.2$
$M_5 = 34 / 2$	$M_8 = 4.1 / 1.4$	$M_8 = 4.1 / 4.2$
$M_6 = 64.6 / 2$	$R_C = 30\text{-K}\Omega$	$M_{Rc} = 300 / 0.7$
$M_7 = 320 / 120$	$C_C = 2\text{-pF}$	$C_C = 164.8\text{-pF}$
$M_8 = 5 / 120$		

Table 3.2 Aspect ratio of the dual-loop TIA

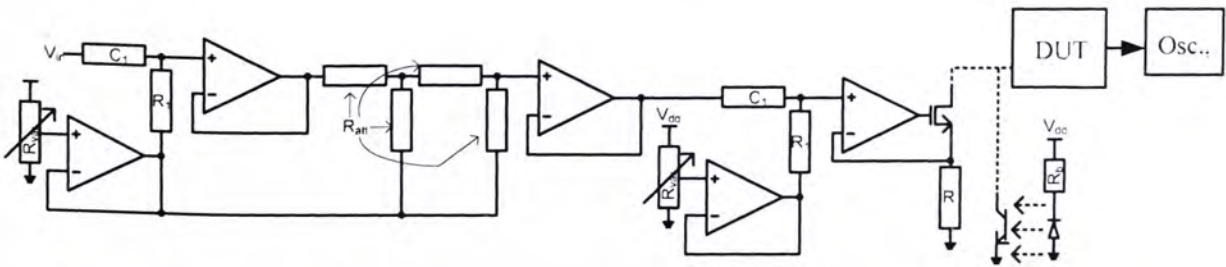


Fig. 3.34 Test fixture for the dual-loop transimpedance amplifier with DC photocurrent rejection.

Measurement result

The lower-band f_{-3dB} in Fig. 3.35 ranges from 372-Hz down to 0.47-Hz, for input DC currents from 110- μ A to 2.7- μ A, respectively. The gain of the TIA is about 63.5-dB, which is consistent with simulation result. The TIA is clearly working as different cutoff frequencies and attenuations are obtained. These waveforms corresponds to the circuit simulation as can be seen from Fig. 3.36, in that the zero generated by the photocurrent rejection loop at 83-KHz and the complex pole generated by Eq. 3.26 at 163-KHz are visible. Also, throughout most of the stopband and passband, the simulation and measurement results are in good agreement within 1-dB of each other, except at higher frequency (great than 20-KHz) where the peaking is severe. Nevertheless, it is not critical for this application since this range lies outside of the operating frequency of the circuit.

Fig. 3.37 is shown to illustrate the relationship between the lower-band f_{-3dB} and DC photocurrent. The circuit can be seen as a bandpass filter with a four orders of magnitude of tuning capability in its lower-band, as controlled by I_{dc} . The extended range of tuning is achieved by transistors in DC current rejection loop operating in the sub-threshold region. Normally, M_1 , M_{ctl} and M_2 operate in saturation region while the rest of the transistors operate in sub-threshold region for $I_{dc} \geq 15 \mu$ A, as shown by the square root relationship between the lower-band f_{-3dB} and DC current ($g_m \propto \sqrt{I_d}$), which implies saturation operation. This makes sense since M_1 , M_{ctl} and M_2 dictate the lower-band f_{-3dB} (see Eq. 3.4). Moreover, M_1 and M_{ctl} operate in sub-threshold region during simulation for $I_{dc} < 15 \mu$ A. In actual operation, M_1 and M_{ctl} are believed to have generated the expected sub-threshold g_m . Conversely, M_2 is standalone in the layout with no other components to track with, its g_m can either be in sub-threshold or strong inversion operation, which is process dependent and cannot be simulated accurately with Spectre. Fortunately, process variation works in our favor and M_2 operates in sub-threshold operation, which leads to the extended tuning range. This can be seen from the inset ($g_m \propto I_d$), which implies sub-threshold operation. Consequently, with this dual-loop technique, an effective capacitance from 1.13-nF to 73.1-nF is implemented to push the pole in Eq. 3.4 to low frequency location (from 0.47-Hz to 372-Hz). A factor of 443.6 times reduction in capacitor size compared with the existing technique using Eq. 3.3!

This phenomenon is justified by $I_{dc} = 2.7 \mu\text{A}$ in Fig. 3.37, in which the experimental result and the analytical plot are in excellent agreement within 1-dB. g_{m2} in this case is 0.82-nA/V , much lower than the lowest g_m in simulation. The analytical plot, as said before, is generated by using Eq. 3.21 and setting all transistors in sub-threshold region with the following g_m :

$$g_m = \frac{I_{ds_wi}}{nV_T} \quad (3.33)$$

where

$$I_{ds_wi} = I_{D0} \frac{W}{L} \exp^{\frac{V_{GS}}{nV_T}} \quad (3.34)$$

n is the sub-threshold slope factor, V_T is thermal voltage, I_{ds_wi} is the sub-threshold drain current and I_{D0} is the characteristic current. More information can be found in the Appendix D.

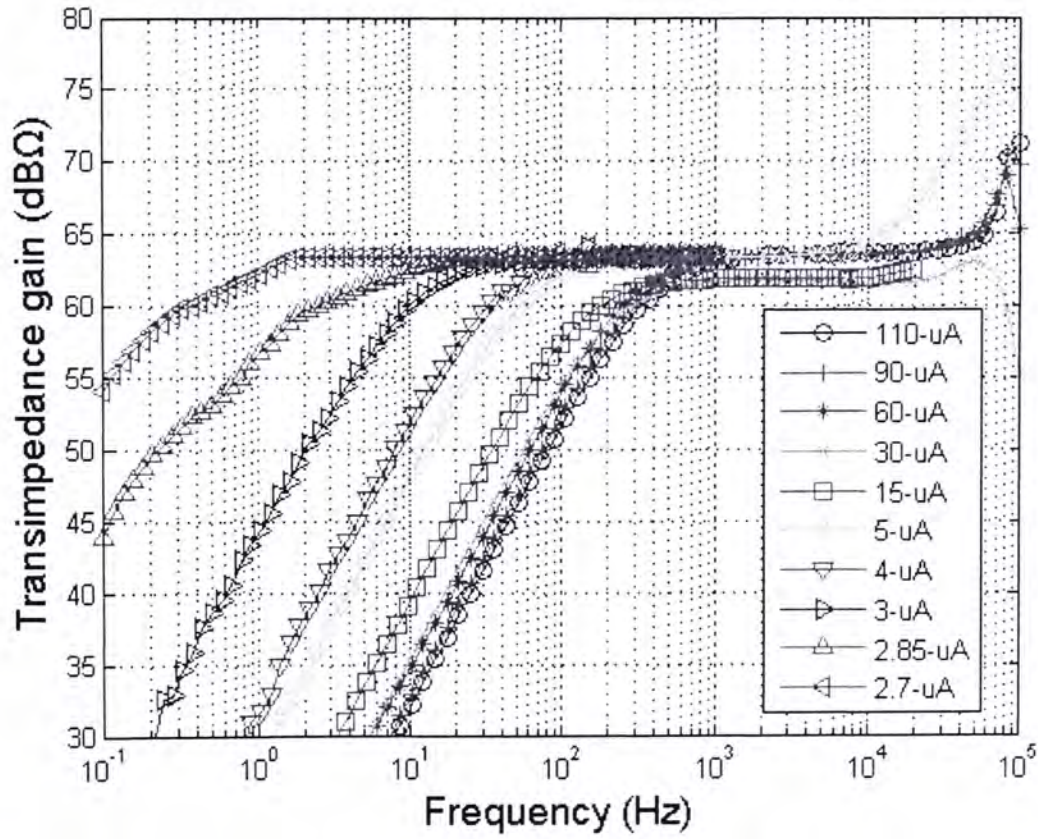


Fig. 3.35 Frequency responses of TIA with various amounts of DC photocurrent, which result in various lower-band f_{-3dB} .

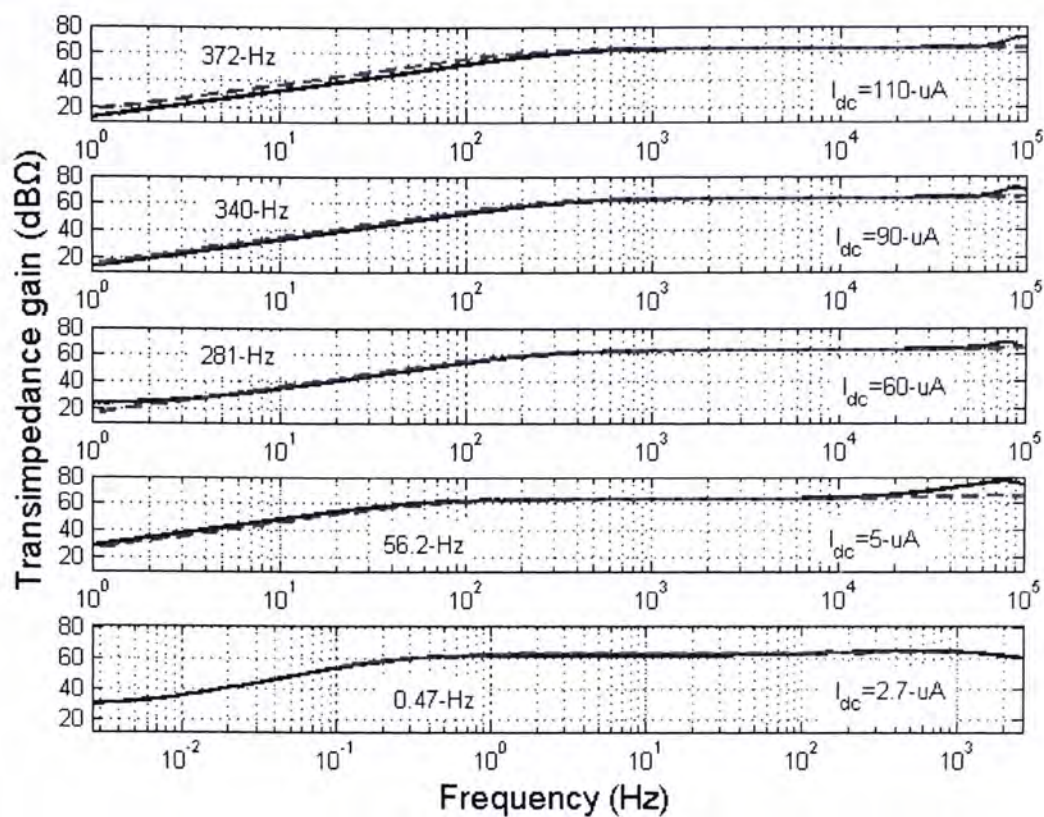


Fig. 3.36 Plot of measured result of frequency response vs. simulated results. Measured result (solid line) and simulated result (dashed line).

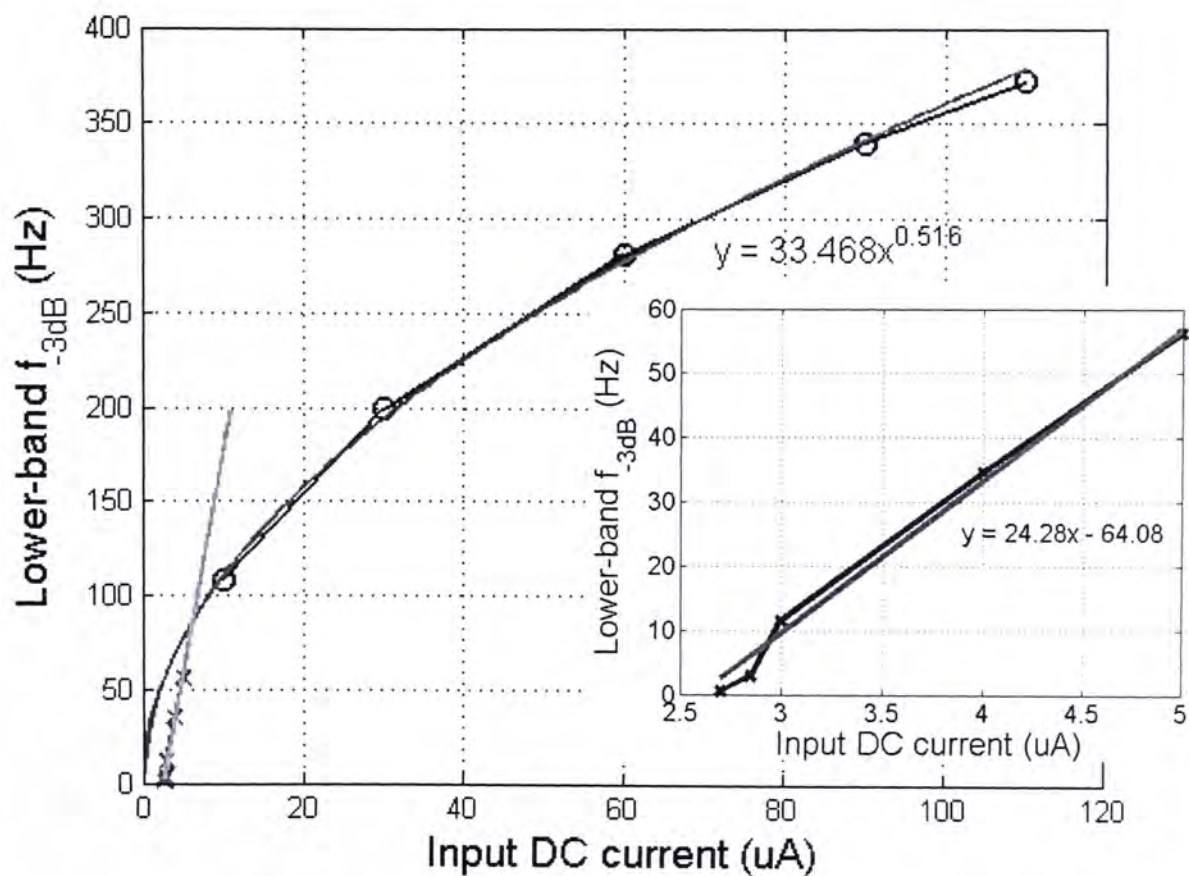


Fig. 3.37 f_{3dB} vs. DC photocurrent. The circuit operates in saturation region for $I_{dc} \geq 15 \mu A$ and sub-threshold region for $I_{dc} < 15 \mu A$. Inset: Zoom-in of linear relationship that provides clue as to the extended f_{3dB} for $I_{dc} \leq 5 \mu A$.

Linearity information is recorded for three different frequencies across different ranges of DC photocurrent. f_{in} of 1-KHz corresponds to audio signal, while f_{in} of

300-Hz corresponds to low frequency neural photonic signal and finally f_{in} of 17-Hz corresponds to physiological signal. For 1-KHz and 300-Hz signal, the linearity information from 110- μ A down to 30- μ A are recorded, and for 17-Hz signal, the linearity information is recorded below 30- μ A because it is assumed the power consumption of LED is reduced.

For physiological signal ($I_{dc} < 20 \mu$ A, and low frequency input – 17-Hz), such as Fig. 3.38, 3.39 and 3.40, since AC current signal does not vary much from person to person, as shown from results in Chapter 4, DR is not important to the application. For small input amplitude, spurious-free dynamic range (SFDR) ≥ 40 -dB is adequate for the front-end since these signals will be lowpass filtered later on.

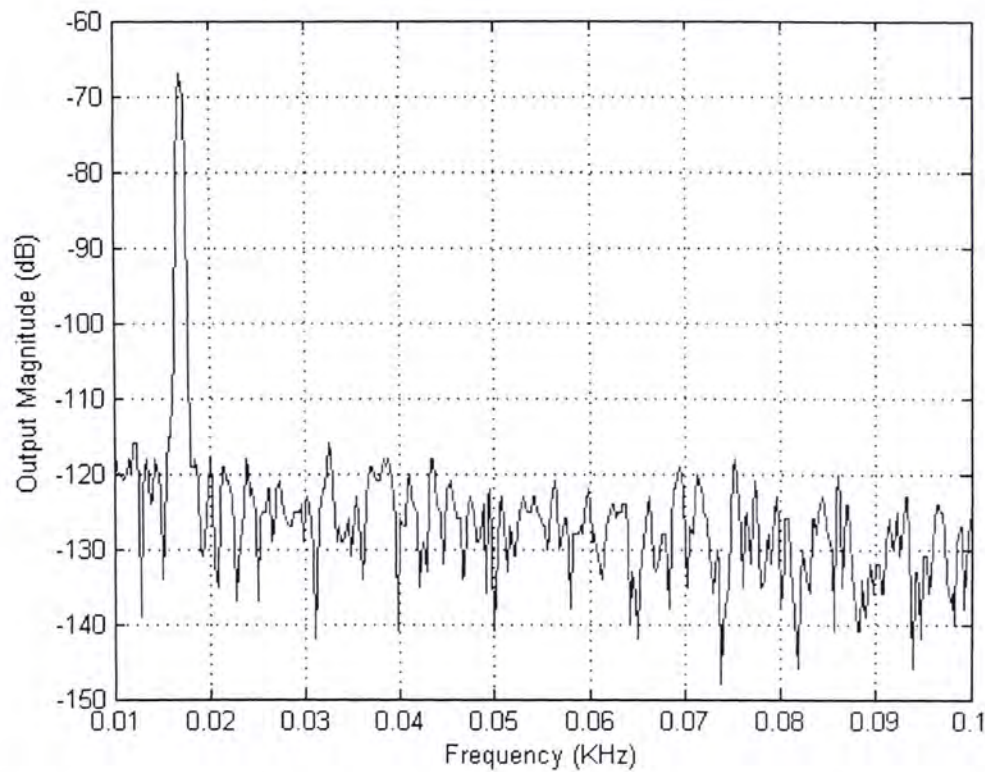


Fig. 3.38 FFT of a 500-nA signal, with $I_{dc} = 5 \mu$ A, $f_{in} = 17$ Hz. The THD is about -49.4 dB (0.34%).

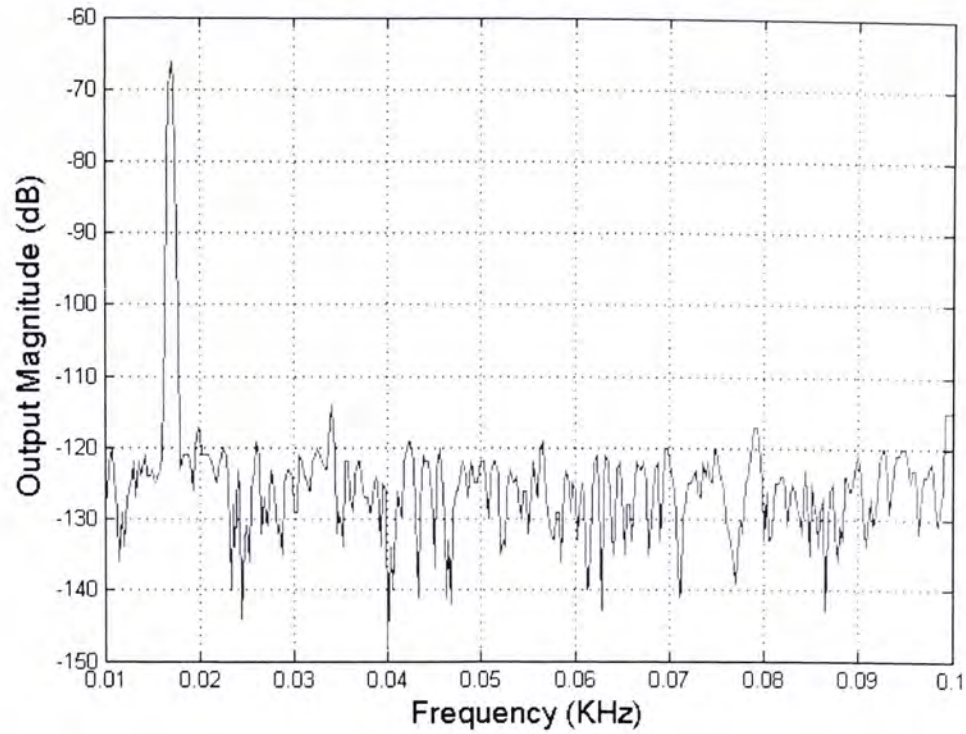


Fig. 3.39 FFT of a 400-nA signal, with $I_{dc} = 2.5 \mu\text{A}$, $f_{in} = 17 \text{ Hz}$. The THD is about -44 dB (0.63%). SFDR: -47.8-dB.

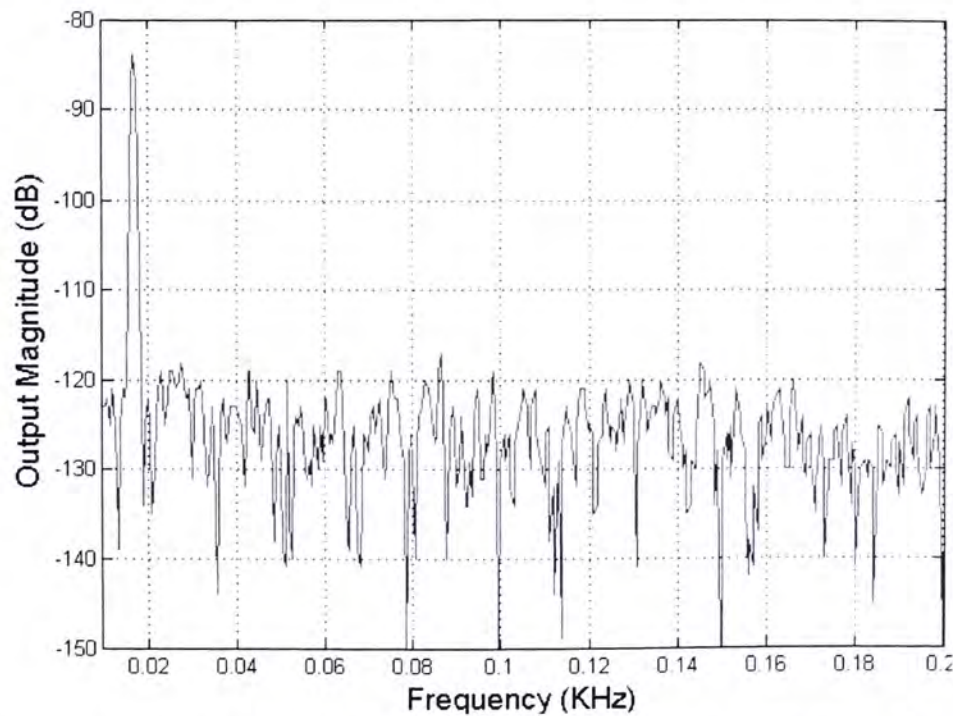


Fig. 3.40 FFT of a 50-nA signal, with $I_{dc} = 2.5 \mu\text{A}$, $f_{in} = 17 \text{ Hz}$. The SFDR is about -33.2 dB.

For neural photonic signal and hearing aid signal ($I_{dc} > 30 \mu\text{A}$, and higher frequency input – 300-Hz and 1-KHz), such as Fig 3.41 and 3.42, both the linearity and DR are important. For Fig. 3.41, the THD is about -48.7-dB for an $I_{pk} = 1.25 \mu\text{A}$, with $I_{dc} = 30 \mu\text{A}$, which is sufficient for this application. The system performs reasonably well for large input signal as well, as can be seen from a SFDR of -48.2-

dB in Fig. 3.42. The THD vs. DC photocurrent for 3 different frequencies is plotted in Fig. 3.43. At in-band frequency (1-KHz), the THD is quite high across all DC current and becomes low at frequency closer to the lower-band f_{-3dB} (17-Hz and 300-Hz). However, if SFDRs are compared, they are almost the same. Probably, the noise floor at 1-KHz is higher than that at 300-Hz due to high frequency component, which contributes to a worst THD. Finally, the SFDR vs. input AC current for $I_{dc} = 30 \mu\text{A}$ is plotted (Fig. 3.44) to illustrate its DR. For a 3% THD, the DR is approximately 50.4-dB. Since the system is not optimized for DR, this result is satisfactory. Both the linearity and DR can possibly be improved by increasing the forward transimpedance gain (R_f) to increase the peak magnitude of the tone (to increase the SNR) and by minimizing the head room in the output stage of the EA to increase swing.

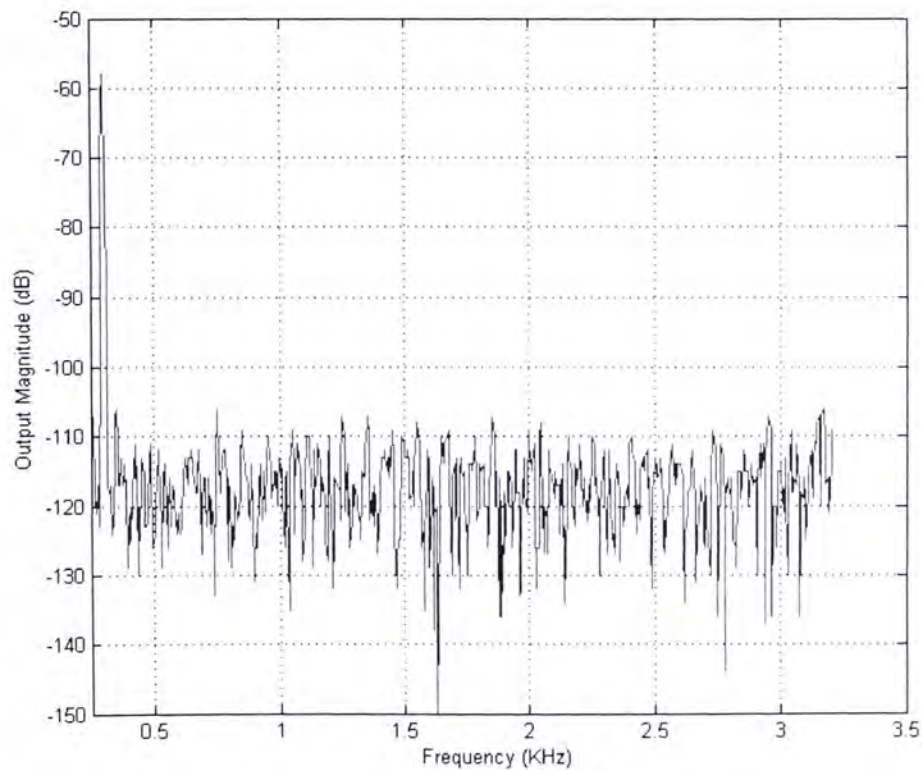


Fig. 3.41 FFT of a 1.25- μA signal, with $I_{dc} = 30 \mu\text{A}$, $f_{in} = 300 \text{ Hz}$. The THD is about -48.7 dB (0.37%).

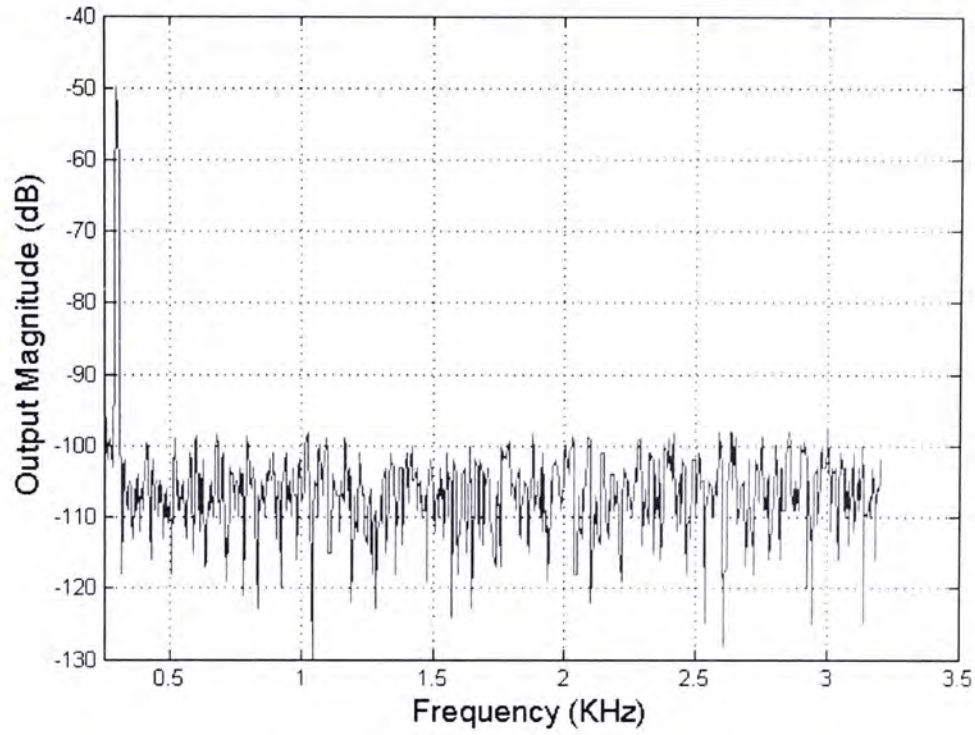


Fig. 3.42 FFT of a 2.56-μA signal, with $I_{dc} = 30 \mu\text{A}$, $f_{in} = 300 \text{ Hz}$. The SFDR is about -48.2 dB. This plot illustrates the FFT response of a 300-Hz neural/audio signal.

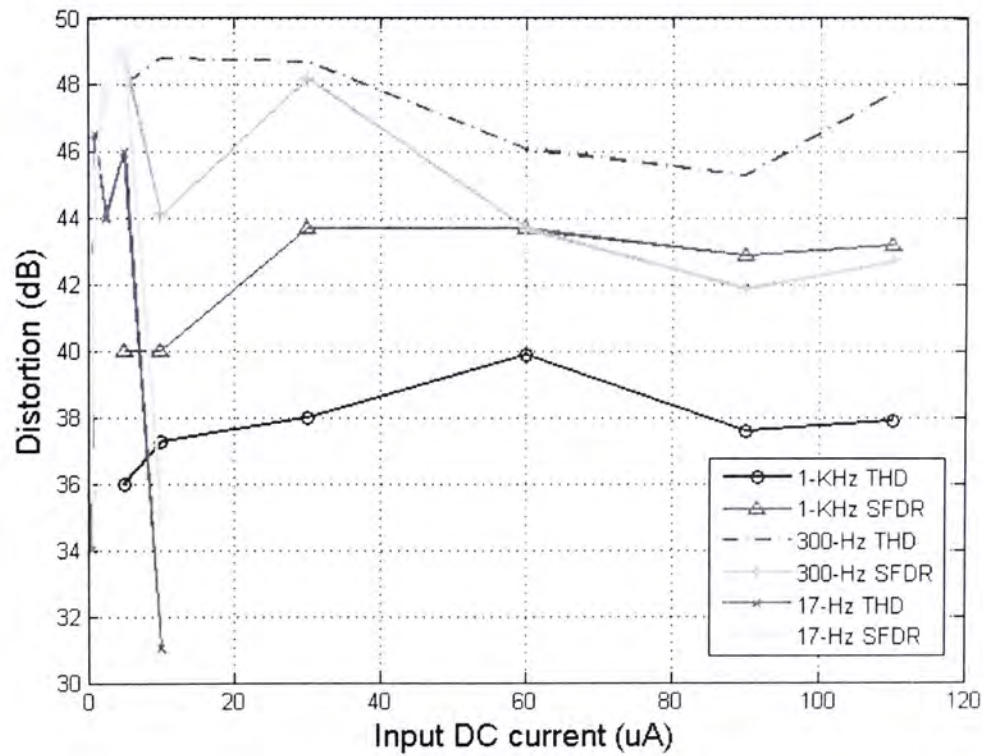


Fig. 3.43 THD vs. input DC photocurrent for input with different f_{in} . For $f_{in} = 1 \text{ KHz}$ and 300 Hz , $I_{inpk} = 1.25 \mu\text{A}$ and for $f_{in} = 17 \text{ Hz}$, $I_{inpk} = 403 \text{ nA}$.

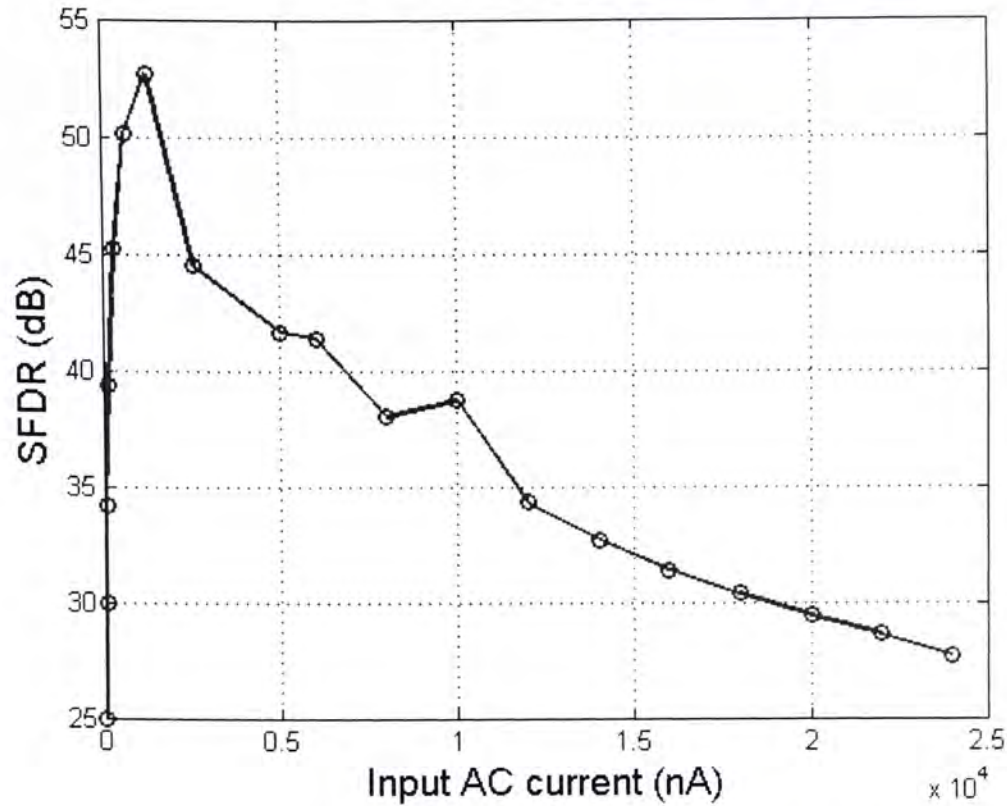


Fig. 3.44 SFDR vs. input to show DR at $I_{dc} = 30 \mu\text{A}$. For a 3% SFDR, DR is about 50.4-dB.

To demonstrate the functionality of the DC current rejection loop and the entire circuit, a sinusoidal current source is fed to node I_{in} of Fig. 3.10 with a variety of I_{dc} . And sinusoidal voltage outputs are recorded in Fig. 3.45a) and b) to confirm consistency and functionality of entire system. f_{in} of signal is about 300-Hz and these signals are filtered off-line again with a cutoff frequency of 400-Hz to remove high frequency noise. Clearly, the circuit is working as all output settles to about 1.251-V. Henceforth, the proposed circuit can remove the DC offset properly and hence increases DR of the system.

Biological test result is also obtained by placing the sensor unit onto the forehead with LED operating at full power ($I_{dc} = 60 \mu\text{A}$) to record hemoglobin oxygenation at the frontal lobe. Since the initial result in Fig. 3.46 is full of high frequency spur, an off-line filter with cutoff frequency of 10-KHz follows the dual-loop TIA to produce this waveform. This is the preliminary step for gathering information used in NIR spectroscopy [30]. The waveform recorded from this circuit matches those obtained from [15].

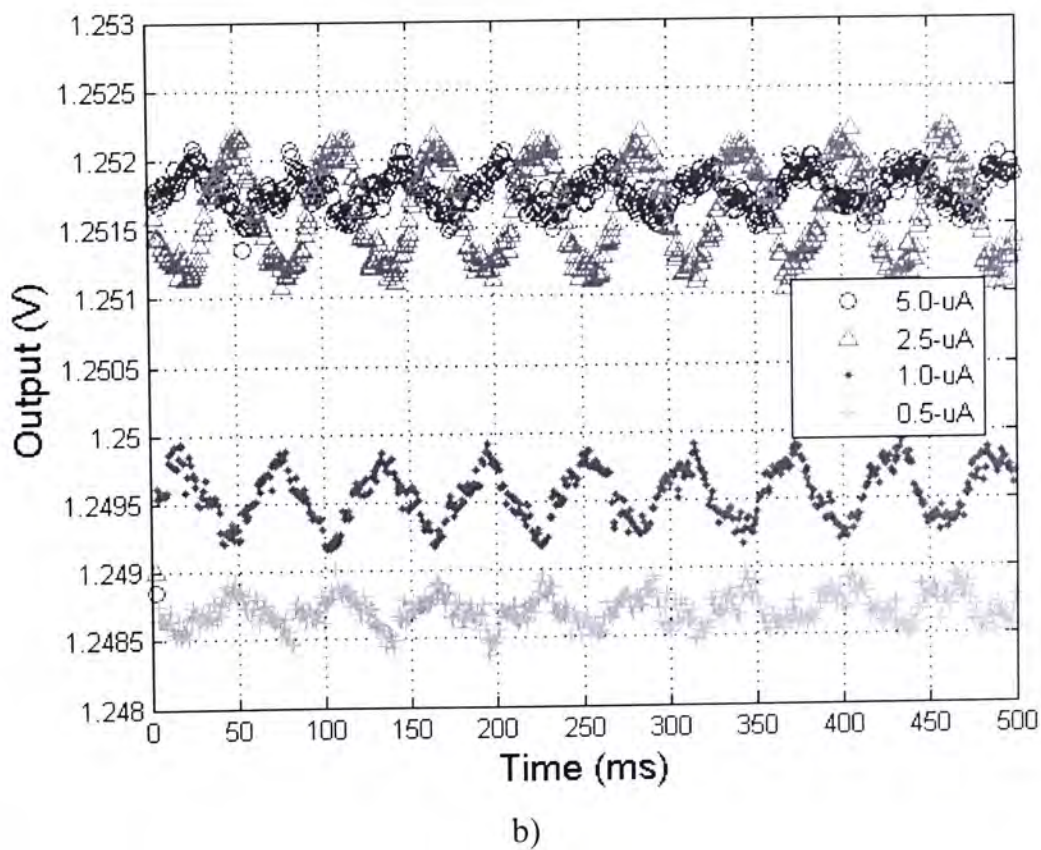
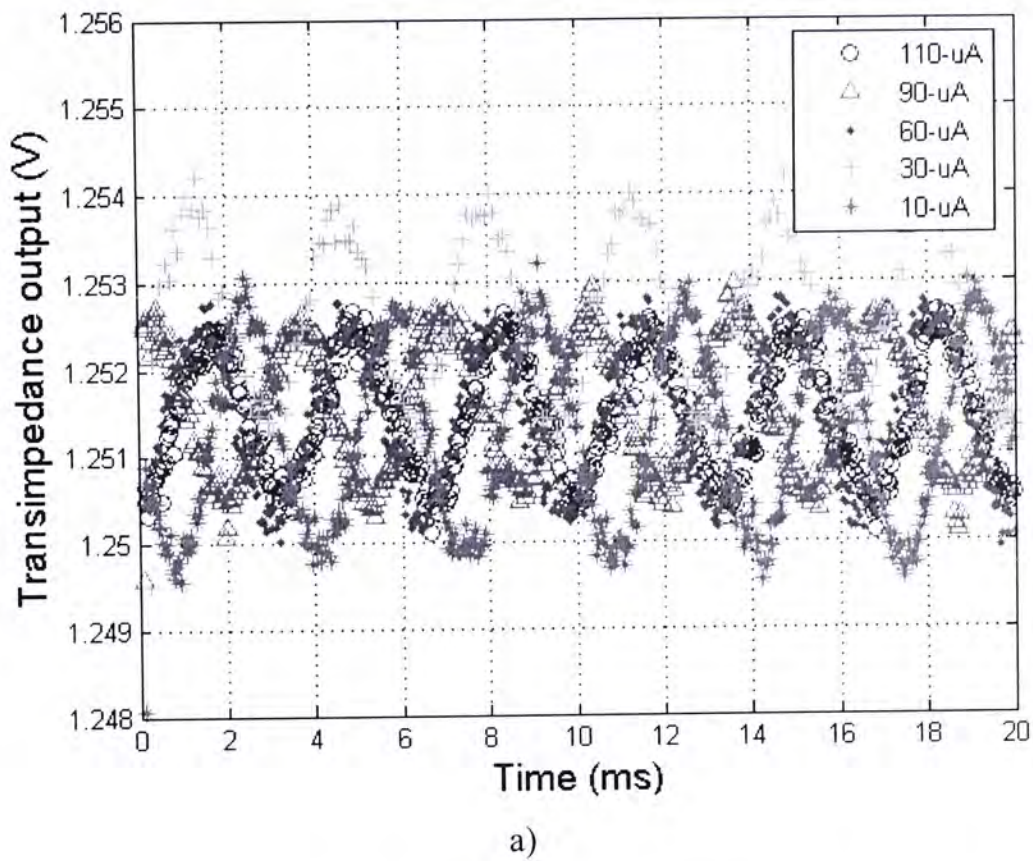


Fig. 3.45 Transient waveforms with different I_{dc} to demonstrate consistency and functionality of system. a) from 10- μ A to 110- μ A, and b) from 0.5- μ A to 5.0- μ A.

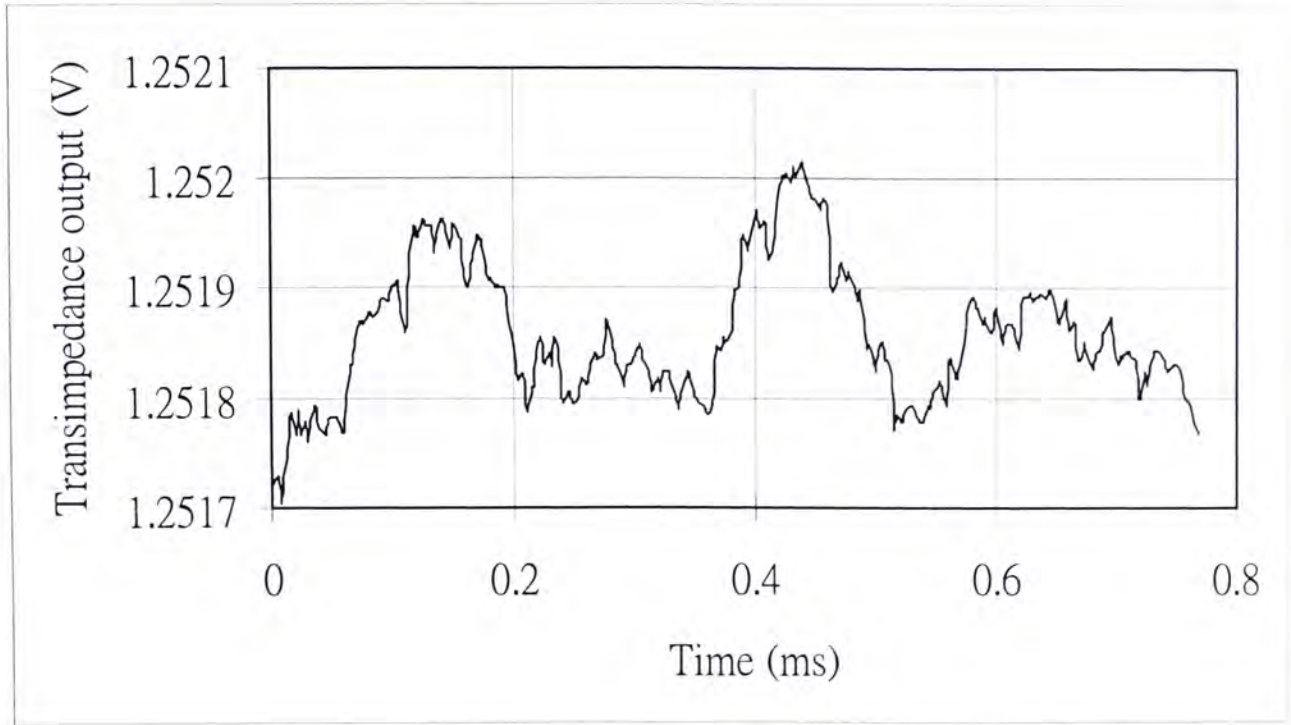


Fig. 3.46 Transient waveform (two periods) – obtained by further filtering the output with 10-KHz cutoff.

The input noise spectral densities of the circuit for two different I_{dc} are shown in Fig. 3.47 and 3.48. Fig. 3.47 corresponds to the noise level of the circuit at $I_{dc} = 5 \mu\text{A}$, whereas Fig. 3.48 corresponds to that at $I_{dc} = 20 \mu\text{A}$. The $1/f$ noise is predicted accurately by simulation, analytical calculation and measurement results. For I_{dc} of $5\text{-}\mu\text{A}$ and $20\text{-}\mu\text{A}$, the input referred integrated current noise from 60-Hz to 5-KHz and 150-Hz to 5-KHz are about $35.6\text{-nA}_{\text{rms}}$ and $34.7\text{-nA}_{\text{rms}}$, respectively. This is adequate since input AC current is typically about a few hundred nano-amperes and sufficient SNR is guaranteed with this figure. This figure can be further improved by increasing C_m , R_f , using PMOS input diff pair for the EA, and maximize the W and L of each transistors to lower the $1/f$ noise. Table 3.3 summarizes the performance of the dual-loop TIA with DC photocurrent rejection.

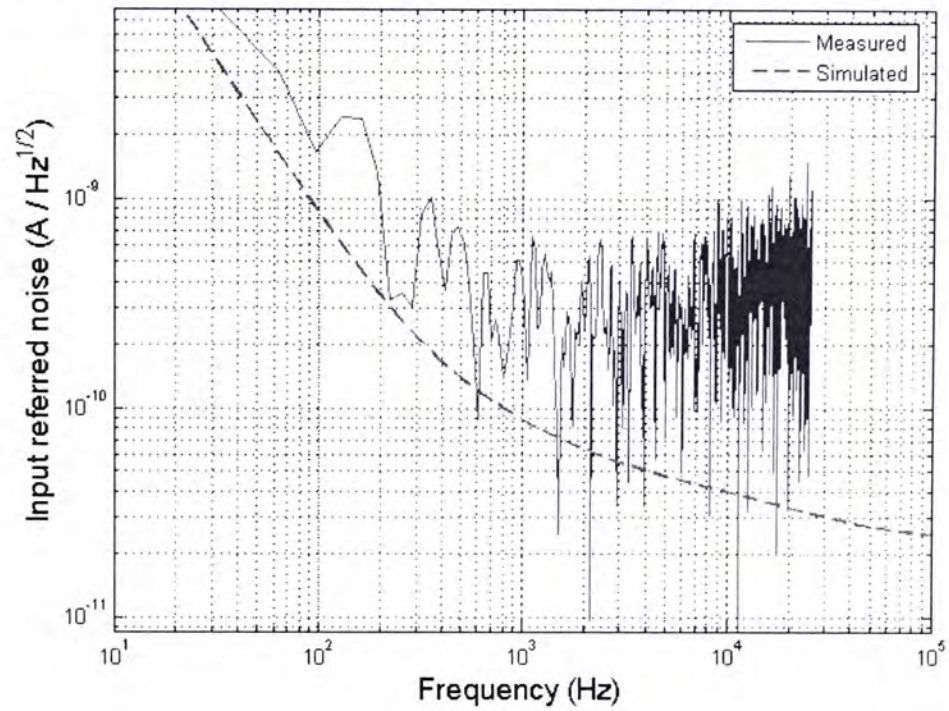


Fig. 3.47 Input noise spectral density (current) of TIA, with $I_{dc} = 5 \mu\text{A}$.

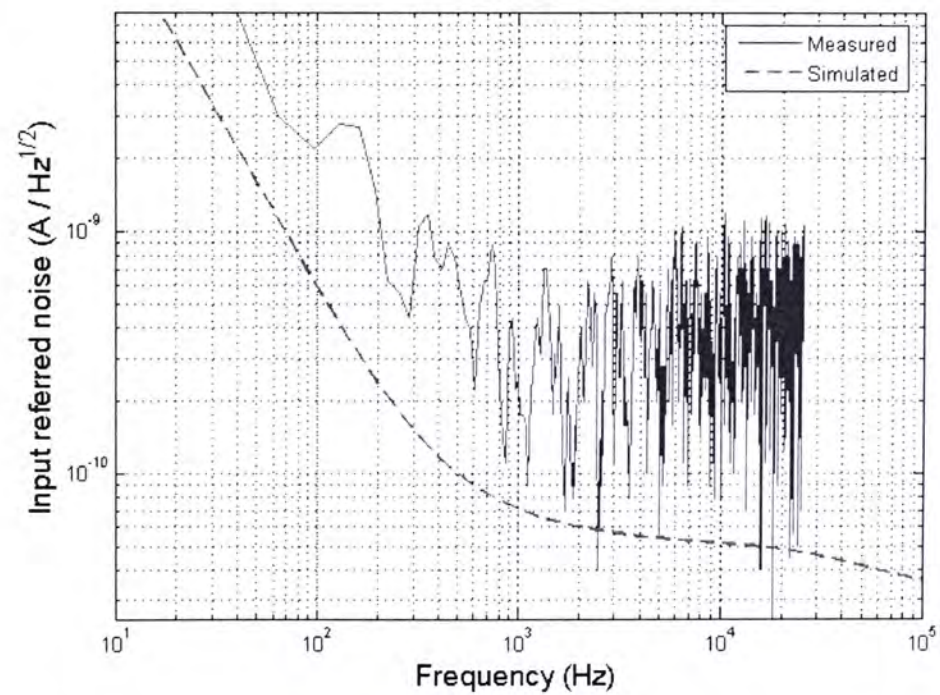


Fig. 3.48 Input noise spectral density (current) of TIA, with $I_{dc} = 20 \mu\text{A}$.

Technology	4M/2P 0.35- μ m CMOS
Supply voltage	2.5 V – 2.0 V
Core circuit area	0.67 mm ²
On-chip capacitance	$C_{p7} = 7.2$ -pF $C_m = 164.8$ -pF
Power consumption	272.5 μ W ($I_{dc} = 60$ μ A) 155.8 μ W ($I_{dc} = 20$ μ A) 111.65 μ W ($I_{dc} = 5$ μ A) 104.3 μ W ($I_{dc} = 2.7$ μ A)
Minimum lower-band f_{-3dB}	0.47-Hz ($I_{dc} = 2.7$ μ A)
Maximum lower-band f_{-3dB}	372-Hz ($I_{dc} = 110$ μ A)
Transimpedance gain	1.6 K Ω
Input Integrated noise (1 to 5-KHz, $I_{dc} = 30$ μ A)	53.6-nA _{rms}
Dynamic Range (3% THD, $I_{dc} = 30$ μ A)	50.4-dB

Table 3.3 Performance summary of the dual-loop TIA.

3.4 Summary and comparison

Two transimpedance amplifier (TIA) ICs fabricated in 0.35- μ m CMOS technology were presented in this chapter. The first one was a TIA with S/H in the feedback loop to perform average level detection of a pulsating PPG signal and rejection of various amounts of DC photocurrent. It achieves a lower-band f_{-3dB} that ranges at about 0.6-Hz. The LED is pulsed at 100-Hz with 10% duty cycle, the sampling period occurs within the LED on time and the hold period is 9-ms. This TIA works properly as the result section has shown. The second one was a dual-loop TIA with DC photocurrent rejection for continuous time multi-parameter (hearing aid, neural photonic and physiological signal) application. It can reject DC current from 2.7- μ A to 110- μ A, and achieves a lower-band f_{-3dB} from 0.47-Hz to 372-Hz without any external components, which is equivalent to 443.6 times reduction in capacitor size. It consumed 155.8- μ W and 109- μ W from a 2.5-V and 2.0-V supplies, respectively. With a 20% reduction in voltage supply, the DC operational range of the dual-loop TIA worsens due to headroom problem in DC cancellation loop and insufficient swing on the part of EA’s second stage in the pole lowering loop. A comparison table with other biomedical front-end designs and capacitance multiplication techniques is summarized in Table 3.4.

To illustrate the efficiency of the Active Miller capacitor multiplication technique of various circuits, a multiplication factor (M-factor) efficiency is computed, which is given by the following:

$$M - Factor \ Efficiency = \frac{power}{Multiplication \ factor}$$

[20], [28], [31] and this work are compared because they require an opamp in feedback loop with very large active Miller component. This shows that our work achieves an M-factor efficiency that is 9.13 times of [31] and 16.3 times of [28]. Although not the best, this is the highest multiplication factor achieved for the amount of current consumed for biomedical application. Thus, this circuit topology is proved to be unique and versatile for NIR sensing application.

The dual-loop TIA with DC photocurrent rejection is the first fully integrated transimpedance amplifier ever presented for biomedical application that accommodates input of diverse nature. It has the widest frequency tuning range, from a few tenths of hertz to hundreds of hertz, in its lower-band f_{-3dB} . While for most of other circuits, the lower-band is fixated by the value of its pseudo resistors [10], [15], [31]-[32]. The circuit's performance is predictable and is less process dependent compared to its pseudo resistors counterpart [15]. The system can operate with a wider range of DC operating points as well compared to [16] and with no external components compared to [32].

Ref.	Technology	Supply voltage	Supply current	Input DC current range	Lower cutoff f_{-3dB}	M-factor efficiency	Input referred noise	THD
[7]	0.35- μ m CMOS	3.00V	2.67 mA	300 nA to 30 μ A	1 MHz	N/A	6.7pA/ $\sqrt{\text{Hz}}$	N/A
[10]	0.18- μ m CMOS	1.80V	166.0 μ A	0.5 μ A to 2.5 μ A	0.3 Hz	N/A	2.2nA (integrated noise)	N/A
[15]	1.5- μ m CMOS	5.00V	16.0 μ A	N/A	0.025 Hz	N/A	2.2 μ V (integrated noise)	1.00%@16.7 mV _{pp}
[16]	1.5- μ m CMOS	2.80V	34.3 μ A	30 μ A	N/A	N/A	10 μ V (integrated noise)	N/A
[20]	N/A	2.50V	50.0 μ A	N/A	N/A	0.08×10^{-6}	N/A	N/A
[28]	1- μ m CMOS	1.25V	30.0 μ A	N/A	N/A	3.75×10^{-6}	N/A	N/A
[31]	0.35- μ m CMOS	3.30V	6.36 mA	Few tens of nA.	100 Hz	2.1×10^{-6}	4fA/ $\sqrt{\text{Hz}}$	N/A
[32]*	0.5- μ m CMOS	3.00V	20.0 μ A	N/A	0.3 Hz	N/A	60nV/ $\sqrt{\text{Hz}}$	N/A
This work	0.35- μ m CMOS	2.50V	73.1 μ A	2.7 μ A to 110 μ A	0.5 to 372 Hz	0.23×10^{-6}	53.6nA (integrated noise)	0.36%@5.12 μ A _{pp}

Remark: 1. $M - \text{Factor Efficiency} = \frac{\text{Power}}{\text{Multiplication factor}}$ (defined by authors; smaller M-factor efficiency is better.)

- 2. N/A = Not Available
- 3. * Using external components

Table 3.4 Comparison of overall system with other works.

CHAPTER 4: ULTRA-LOW CUTOFF FREQUENCY FILTER

DESIGN

In this chapter, we present an ultra-low cutoff frequency filter using current steering technique (CST) that fulfills the requirement in Chapter 2: accurate f_{-3dB} , compact and reasonable power consumption. To verify the functionality of the proposed circuit, this lowpass filter is realized and become part of the signal processing chain, together with the off-chip capacitor TIA in Chapter 3 to form a complete physiological signal (such as PPG) acquisition system. Simulation, measurement and experimental results will be presented.

4.1 Current-steering lowpass filter (CS-LPF)

To arrive at a lowpass filter architecture with ultra low cutoff frequency, robust performance and compactness, active-RC implementation is preferred. Fig. 4.1 is an R-MOSFET-C filter from [26], which satisfies this requirement for adaptation. This fully-differential filter structure is part of the 22-KHz fifth-order Bessel filter for audio application. Not only does this filter exhibits low distortion because of the current-steering transistor inside the feedback loop, but also it has the potential to be realized as a tunable filter with the current division network [25], and evolves to an ultra-low cutoff frequency filter [21], thanks to the pair of current-steering transistors.

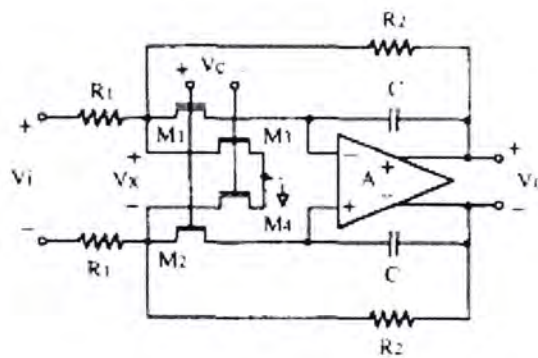


Fig. 4.1 R-MOSFET-C first order filter.

The architecture of the first order CS-LPF is given in Fig. 4.2a together with the α block in Fig. 4.2b. The actual implementation is shown in Fig. 4.3. For our

application, only single-ended version is sufficed. The new transfer function is given by the following:

$$A(s) = \frac{-R_f/R_i}{1 + s R_f C/\alpha}, \quad (4.1)$$

where $\alpha \leq 1$. Therefore, the -3-dB frequency is

$$f = \alpha / 2\pi R_f C \quad (4.2)$$

α is given by:

$$\sqrt{\alpha} = \sqrt{\left(\frac{I_{d1}}{I_{d2}} \right)} = \frac{V_{gs1} - V_t}{V_{gs2} - V_t} \quad (4.3)$$

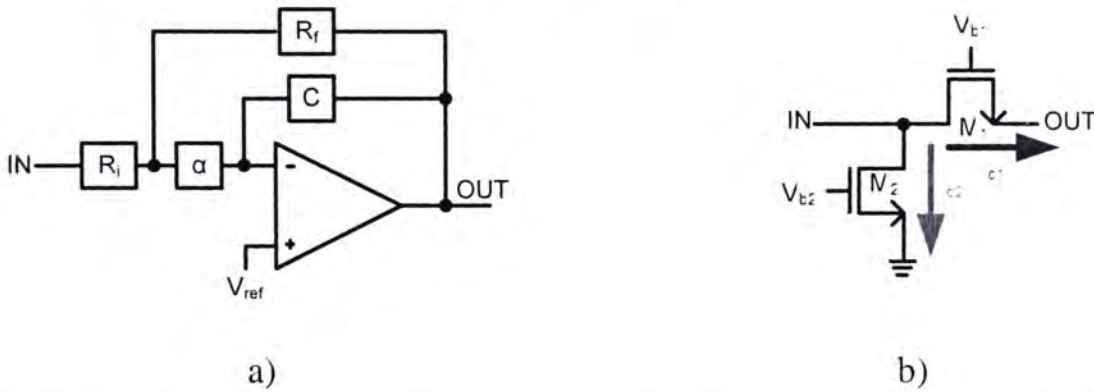


Fig. 4.2 a) Top level of schematic of CS-LPF, and b) schematic of α block.

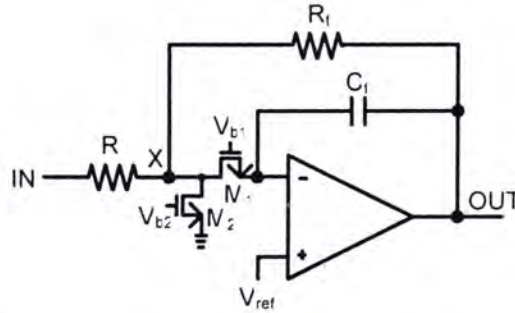


Fig. 4.3 Actual implementation of CS-LPF.

The α section consists of two transistors, which operate at the triode region and act as linear resistors, with identical aspect ratios but different gate voltages to steer current. From Eq. 4.3, frequency tuning is achieved by varying the gate voltage, which in turn steers the currents that flow from the capacitors to virtual grounds, and with this adjustment of gate voltage, the compensation for different process and temperature variations is also achieved. By directing less AC current to the feedback capacitor, the effective capacitance seen at the non-inverting terminal of the opamp is increased by a factor of α . With this technique, a 38-pF capacitor and 17.5-dB gain is

implemented to achieve a cutoff frequency from 62-Hz to 1.8-Hz (and even lower) – an effective capacitive reduction from 500 times to 12,500 times! Nonetheless, for the α block to work properly, its location must precede a high impedance node such that the AC current would only flow to the ground or the feedback capacitor, and node X in Fig. 4.3 would act as the new virtual ground. Again, the opamp is a two-stage configuration in [27], with aspect ratio identical to the TIA opamp in Table 3.2.

The performance of this filter is crucial in alleviating the size of C_H in the TIA and is very robust under different supply voltages, as shown in the experimental section. One short-coming with this filter is its active-RC configuration, which necessitates a buffer in its opamp to provide proper loading for next stage. Another one is that, there is linearity problem as the current steering transistors exhibit non-linearity because the voltages vary at its gate and source as cutoff frequency decreases. Nonetheless, care should be taken in choosing V_{b1} , V_{b2} , cutoff frequency and the aspect ratio of transistors so that the transistors do not operate in the non-linear region of the I_{ds} - V_{dsat} characteristic curve. The main parameters for CS-LPF are summarized in Table 4.1.

Frequency cutoff	1.8-Hz – 62-Hz
(W/L) $M_{1,2}$	0.8- μm / 80- μm
C_f	38-pF
R_i and R_f (K Ω)	7 (R_i), 11.2, 73.2, and 184.8
Effective capacitance	48.6-nF - 1.68- μF
Gain setting	3.5, 17.5 and 28.4 dB

Table 4.1 Main parameters of CS-LPF

4.2 Implementation, experimental and measurement results

In this section, the implementation details, measurement and experimental results from the CS-LPF and the overall system are presented. To verify the functionality and the performance of the CS-LPF, the filter has been integrated as part of the PPG signal acquisition system. First the measurement results of the filter is given, and then followed by that of the overall system.

The micrograph of the overall system is shown in Fig. 4.4. The size of the CS-LPF is about 332- μm by 228- μm and occupies an area of about 0.076-mm². It operates from a 2.5-V supply and consumes about 78.9- μW of power. Extra care is taken in laying out the current steering transistors M_1 and M_2 such that they are matched and

the signal paths that enter and exit the components are about equal, to minimize non-linearity. The test fixture in Fig. 3.28 is used for measurement.

4.2.1 Measurement results for CS-LPF

The measured frequency responses of the CS-LPF with different values of V_{b1} ($V_{b2} = 0.74\text{-V}$) are plotted together with its simulated response in Fig. 4.5. The current steering transistors would work as long as M_2 is in saturation and f_{-3dB} can be varied through adjusting V_{b1} of M_1 . The f_{-3dB} varies from 1.8-Hz to 62-Hz with V_{b1} varies from 1.9-V to 2.1-V. The robustness of the current-steering transistors is clearly seen by the adjustability of f_{-3dB} . From Fig. 4.5, the measurement result deviates significantly from the simulated result (from 1.64 times to 3.34 times) as cutoff frequency decreases. Possibly, at lower cutoff frequency, the operation of M_1 of the current steering transistors is highly non-linear and might be in cutoff due to very small V_{gs} . Since M_1 is located between the virtual ground and the inverting input of opamp, any small variation in its source voltage can change r_{ds} a lot from simulation.

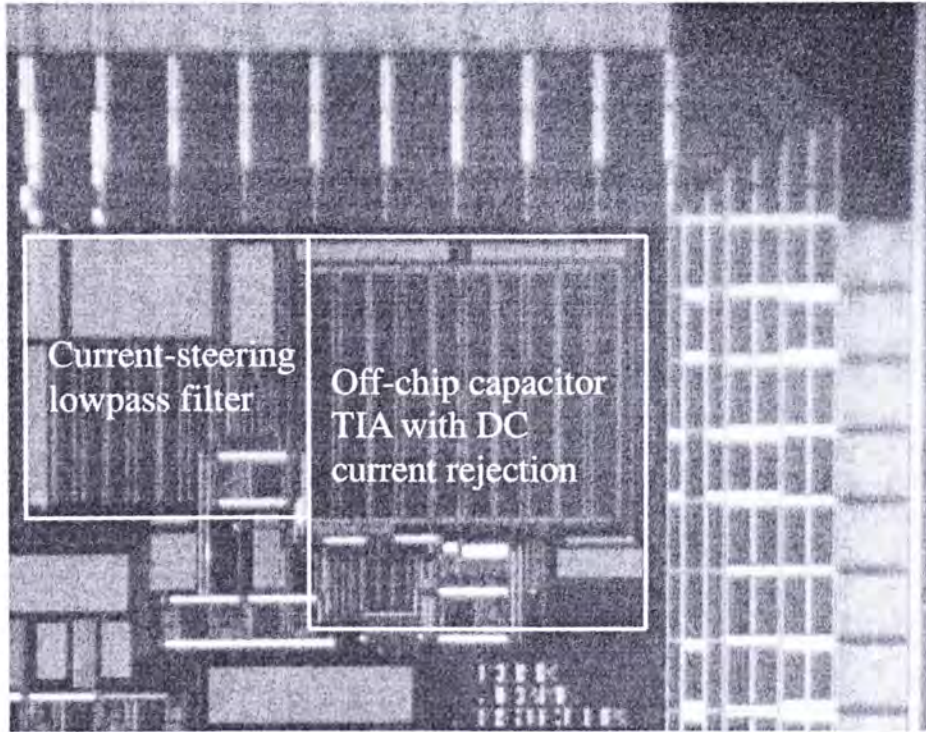


Fig. 4.4 Micrograph of the PPG AFE.

Figs. 4.6, 4.7 and 4.8 show the THD of the filter with f_{-3dB} of 3.1-Hz, 5.67-Hz and 16.4-Hz with 100m-V_{in-pp} to be -33-dB, -47.1-dB, and -50.6-dB, respectively. This is more than enough for our application and the proposed design has not been optimized with respect to this issue. The distortion as a function of cutoff frequency

is plotted in Fig. 4.9. The THD and SFDR are identical at low cutoff frequency and deviate at higher frequency ($f_{-3dB} > 3.1$ -Hz). This is due by non-linearity at low cutoff frequency, which results in strong influence of harmonic tone; whereas there are multiple tones of distortion at very low magnitude compared to the fundamental due to less distortion at higher cutoff frequency. The worst case distortion is at f_{-3dB} of 1.57-Hz, which is about 30.1-dB.

The noise spectral densities for different cutoff frequencies are plotted in Fig. 4.10, 4.11 and 4.12. The input integrated noises are 235.9, 285.9 and 282.7- μV_{rms} for f_{-3dB} of 1.57, 5.67 and 16.4-Hz, respectively. The increase in integrated input noise corresponds to an increase in bandwidth, which is illustrated in Fig. 4.13. These figures are reasonable since this filter is located at the back-end and the input signal power to the filter is much larger than the integrated noise.

Next, the signal-to-noise plus distortion ratio (SNDR) as a function of the input voltage is plotted in Fig. 4.14 to illustrate (DR). With f_{-3dB} of 5.67-Hz and 1.57-Hz, the DRs are about 54.5-dB and 46.6-dB, respectively. The comparison with previous works is summarized in Table 4.2. This filter has the lowest f_{-3dB} ever implemented with active-RC technique.

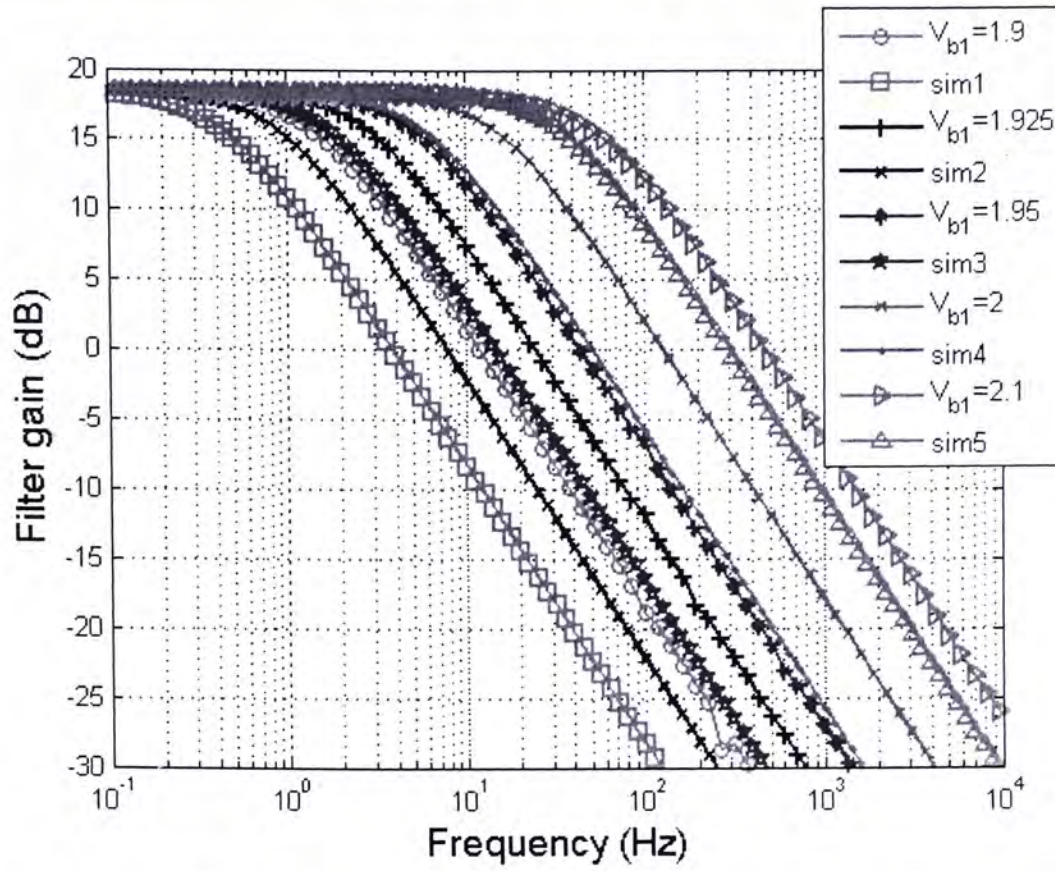


Fig. 4.5 Simulated and experimental frequency responses of the CS-LPF are plotted together.

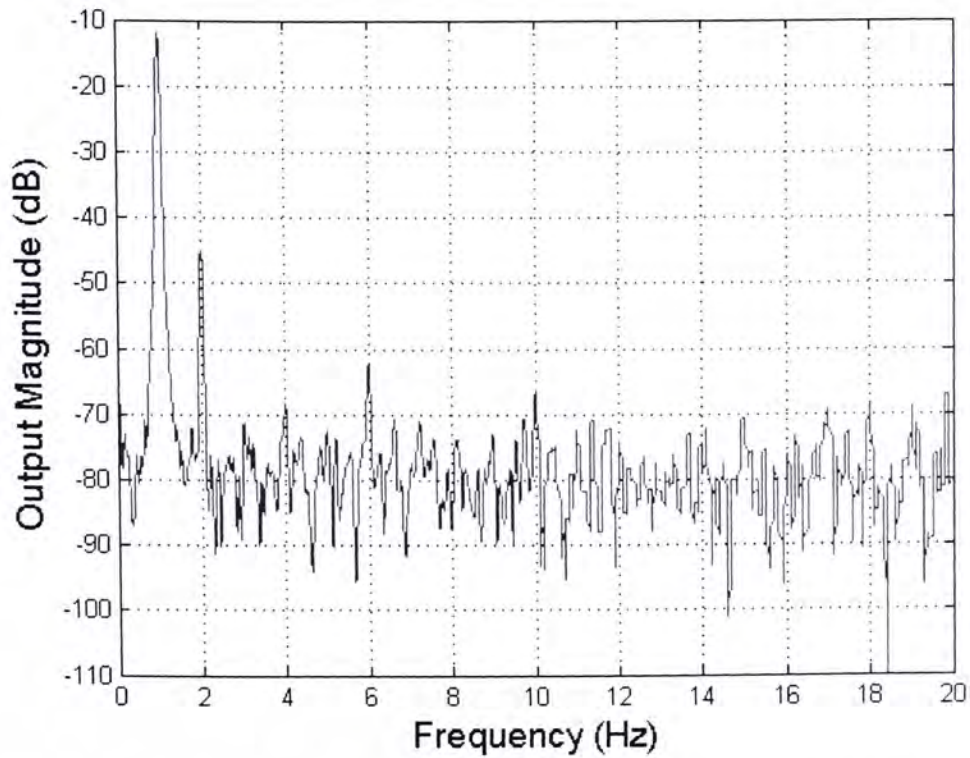


Fig. 4.6 FFT of a 1-Hz signal with $V_{pp} = 100$ mV and f_{-3dB} of 3.1-Hz. SFDR is about -33-dB.

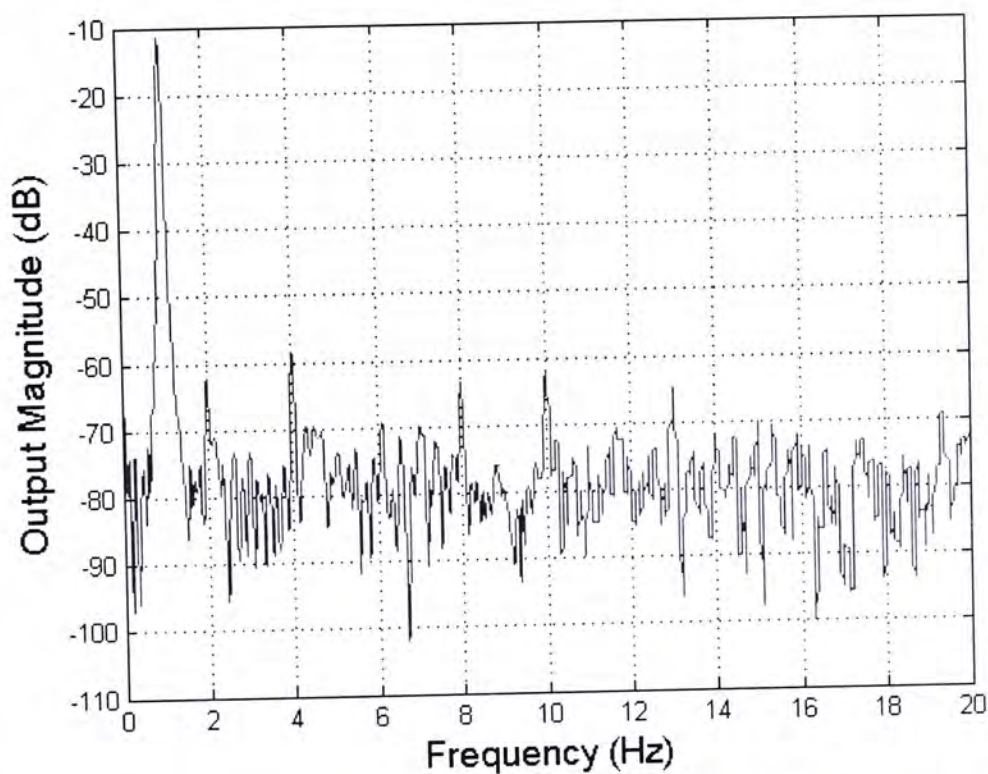


Fig. 4.7 FFT of a 1-Hz signal with $V_{pp} = 100$ mV and f_{3dB} of 5.67-Hz. SFDR is about -47.1-dB.

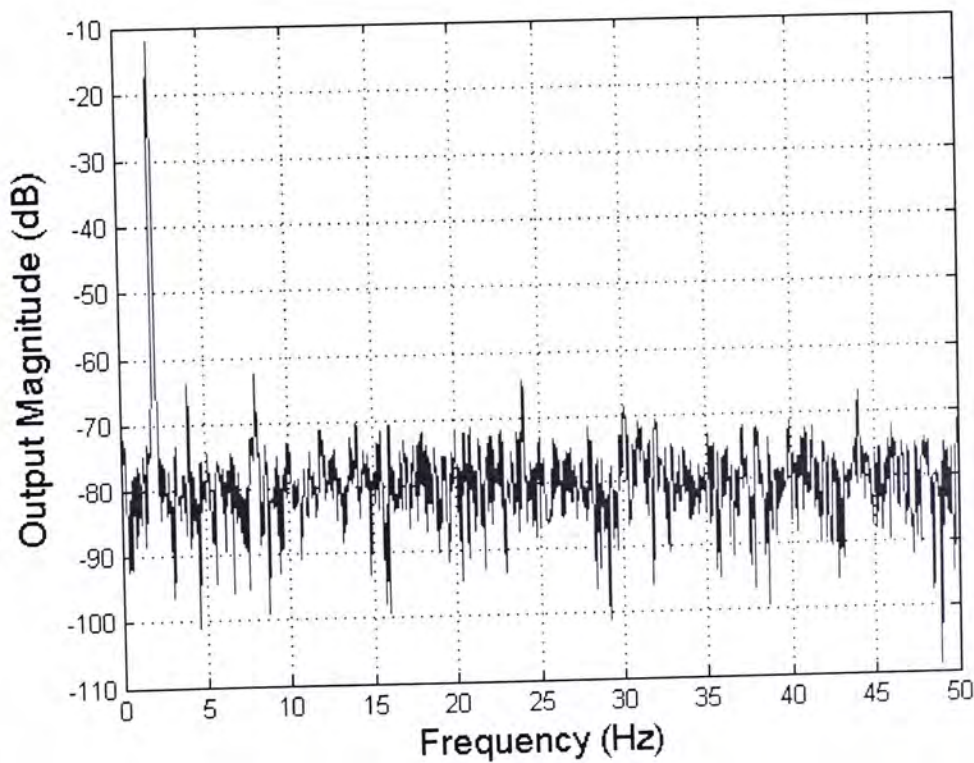


Fig. 4.8 FFT of a 1-Hz signal with $V_{pp} = 100$ mV and f_{3dB} of 16.4-Hz. SFDR is about -50.6-dB.

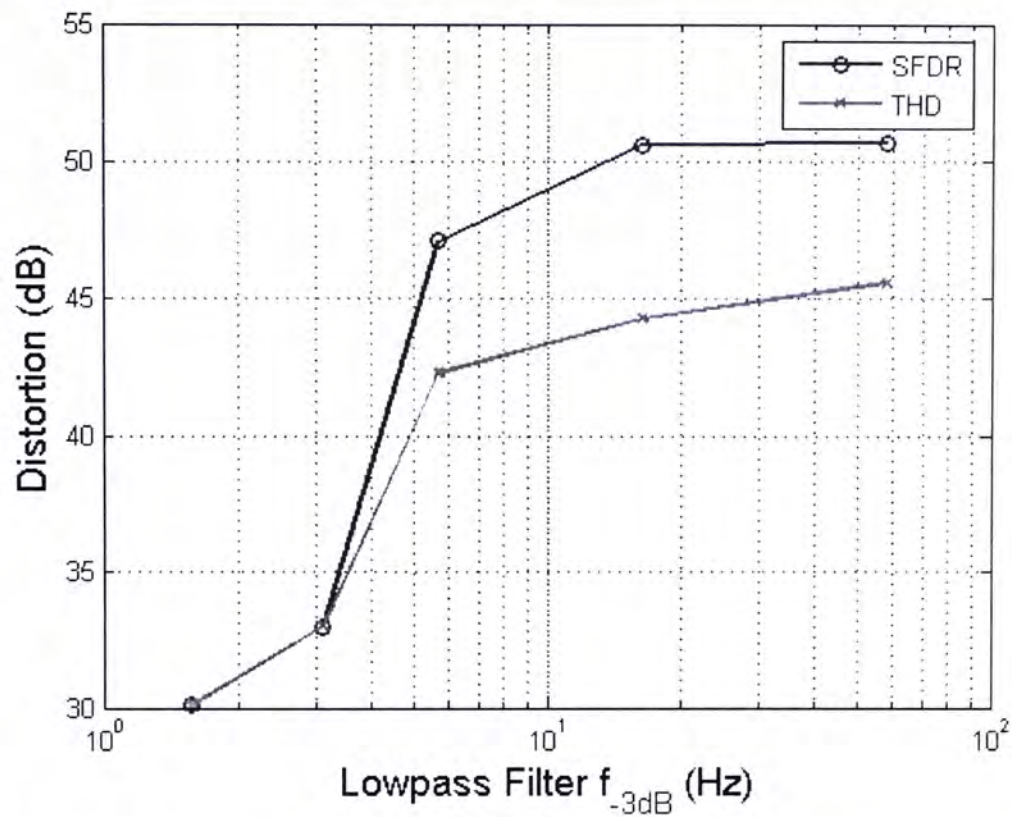


Fig. 4.9 Distortion vs. f_{-3dB} of CS-LPF. The distortion is worst at low frequency due to non-linearity of M_1 .

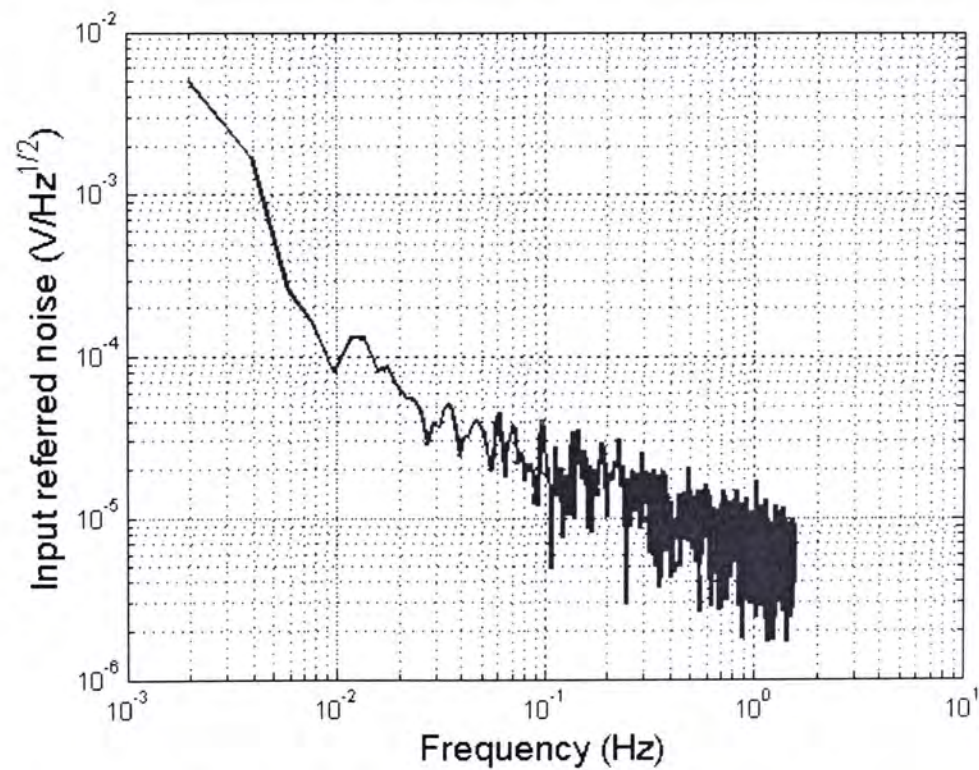


Fig. 4.10 Noise spectral density of CS-LPF at f_{-3dB} of 1.57-Hz. Integrated noise from 0 to 1.58-Hz is $235.9-\mu V_{rms}$.

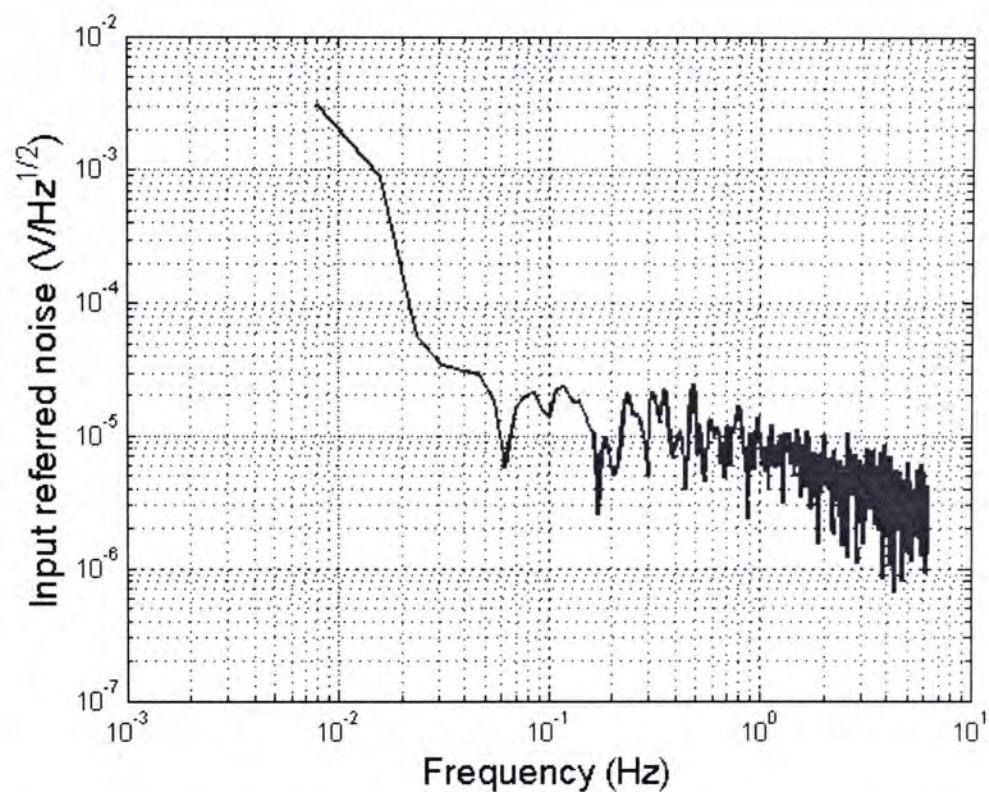


Fig. 4.11 Noise spectral density of CS-LPF at f_{-3dB} of 5.67-Hz. Integrated noise from 0 to 6-Hz is $285.9\text{-}\mu\text{V}_{\text{rms}}$.

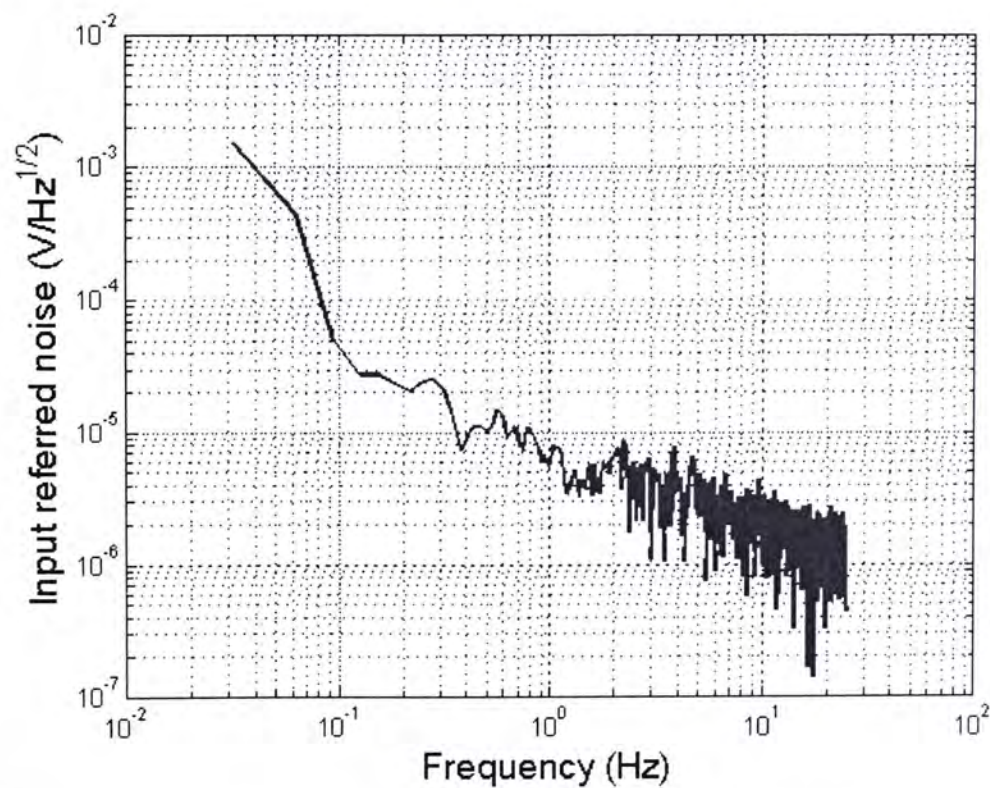


Fig. 4.12 Noise spectral density of CS-LPF at f_{-3dB} of 16.4-Hz. Integrated noise from 0 to 17-Hz is $282.7\text{-}\mu\text{V}_{\text{rms}}$.

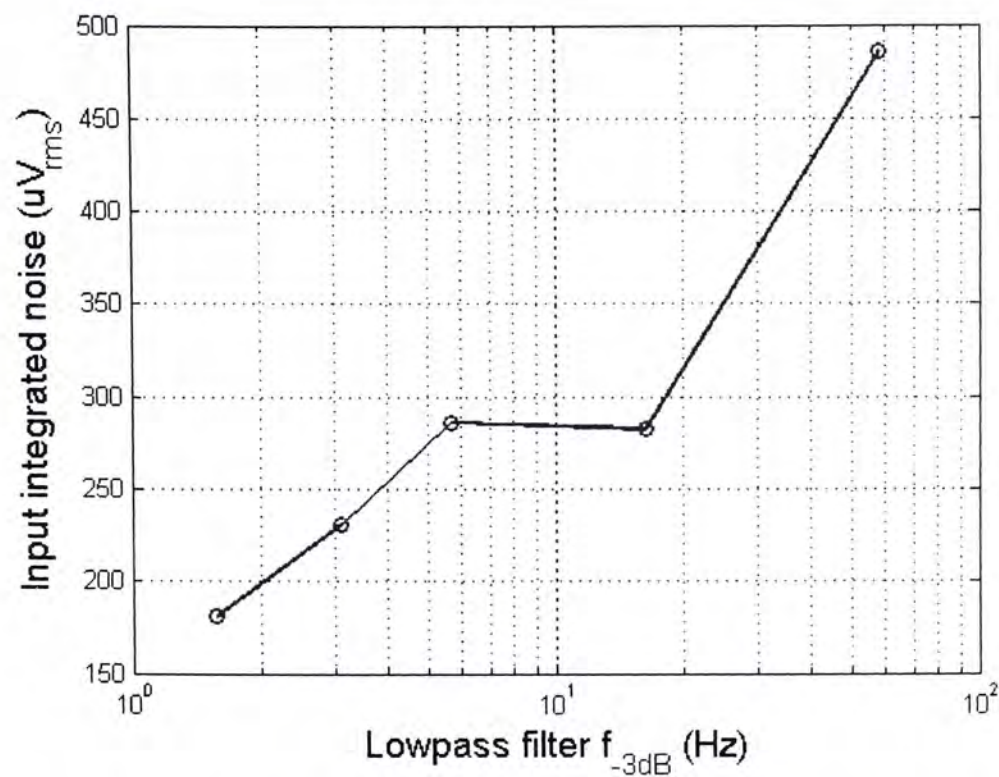


Fig. 4.13 Input integrated noise of filter vs. f_{-3dB} . The noise is higher at larger f_{-3dB} due to wide bandwidth.

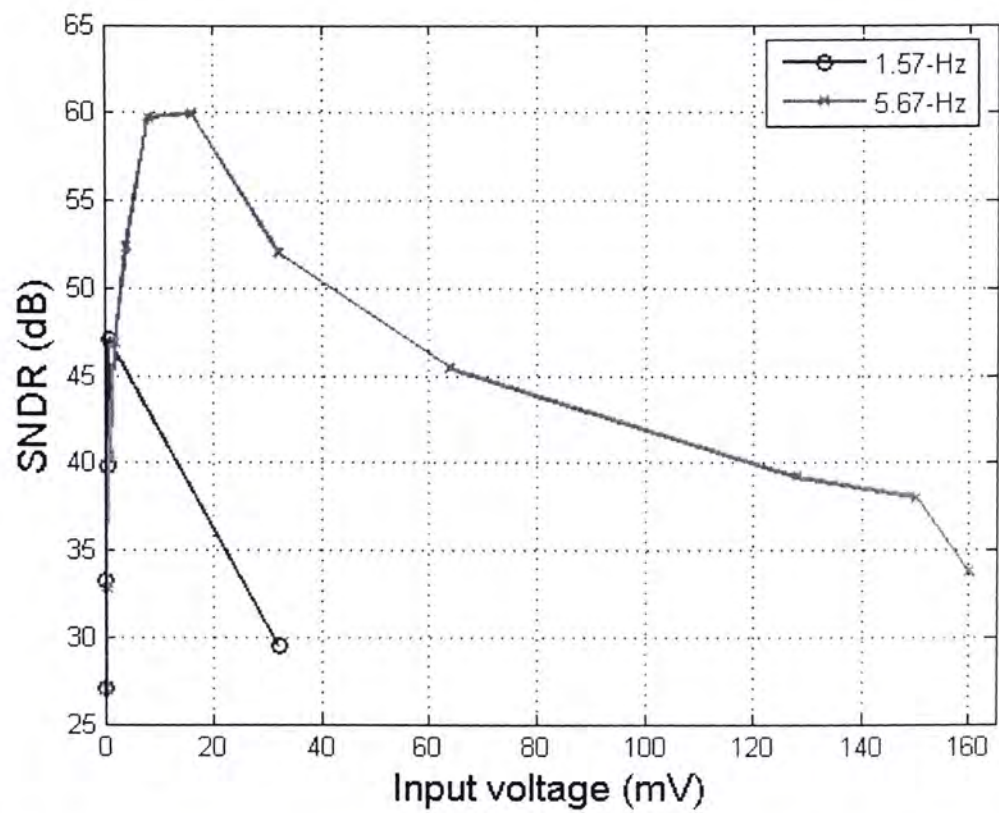


Fig. 4.14 Dynamic range of filter. For a 3% THD, the DRs of the filter are about 54.5-dB and 46.6-dB for f_{-3dB} of 5.67-Hz and 1.57-Hz, respectively.

Reference	V_{supply}	f_{cutoff}	Power (W)	Integrated Noise (V_{rms})	DR (THD)	Technique
[22]	$\pm 1.5\text{-V}$	2.4	$10\ \mu$	50μ (in)	60 dB (0.3%)	G_m -C, cap multiplier
[33]	2.8-V	110	5.1μ	36 pA	50 dB (3%)	G_m -C
[34]	2.8-V	100	230 n	776μ (in)	65 (5%)	G_m -C
[35]	$\pm 1.5\text{-V}$	0.016	0.23μ	-	-	G_m -C
[36]	0.9-V	100	0.5μ	-	45 (1%)	SO-SC
This work	2.5-V	<1.57	78.9μ	235.9μ (in)	54.5 (3%)	Active RC

Table 4.2 Comparison of CS-LPF with other works.

4.2.2 Measurement results for overall system

The frequency response of the entire system with different I_{dc} is shown in Fig. 4.15. The circuit achieves 47.7-dB attenuation for a photocurrent of 20- μ A with an f_{-3dB} lower-band and upper-band of around 0.46-Hz and 2.8-Hz. The range of DC photocurrent that can be sunk effectively while maintaining the desired frequency response is from 0.1- μ A to 53- μ A. Theoretically, the larger the amount of DC photocurrent, the higher the attenuation, but practically this might cause transistors in the error amplifier to go into linear region, which leads to the reduction in attenuation at higher current.

The DC attenuation with respect to passband gain as a function of input DC photocurrent is shown in Fig. 4.16. An in-band (maximum) and stop-band (minimum) signal tones with small enough amplitude are used for calculating the attenuation. This plot demonstrates the DC rejection capability of the system in the presence of various amount of DC photocurrent. The common-mode dynamic range (CMDR), which is defined as the ratio between the maximum and the minimum DC current that achieves at least 20-dB attenuation at its lower stop-band with respect to its passband in the frequency response, is 53-dB (from 0.1- μ A to 53.4- μ A). This means that the system can operate with a LED duty cycle from 0.2 percent to 70 percent, which is very robust and sufficient for our application. The CMDR is dictated by the lower frequency pole (ω_{HP}) and is related to the off-chip compensation capacitor (C_m), which can be integrated later in future development [20], [28].

The transient waveform of node V_{out} in Fig. 3.3a and its FFT are given in Fig. 4.17, 4.18, and 4.19, respectively. In Fig. 4.17, the inputs to the system are in-band

sinusoidal current with various amount of DC current (I_{dc}) from 0.1- μ A to 43.9- μ A, in order to demonstrate the system's ability to reject DC current. The DC level of the output waveforms settles to 1.64-V. There is a discrepancy between the simulation and experimental results due to an offset of 3 to 4 mV at the output of the TIA, which causes the output DC level to be about 400 mV higher than expected. Conversely, this is minimal compared to the rise of DC level if no DC rejection mechanism is presented. For instance, a signal with I_{dc} of 34.6- μ A gives a 10.96-V rise at its output level ($34.6\text{-}\mu\text{A} \cdot 2000 \cdot 20 \cdot 7.5 = 10.96\text{-V}$). Fig. 4.18 shows the FFT of the overall system with a 0.85-Hz in-band tone with I_{dc} of 5- μ A and signal current I_{pk} of 324-nA. The SNDR is about 37.7-dB, which is acceptable for our application. For a signal with I_{pk} of 3- μ A and I_{dc} of 43.9- μ A, the SNDR is 25.3-dB from Fig. 4.19.

The DR of the overall system is shown in Fig. 4.20. The DR is about 29.8-dB for a 5% THD. The DR in this case is limited by the TIA, due to its small amplification factor and poor SNR. In addition, at higher signal current the distortion is severe due to the small input bias current, which is only 3- μ A. Still, the DR is not important since the amplitude of the signal of interest (PPG) does not vary by a large degree.

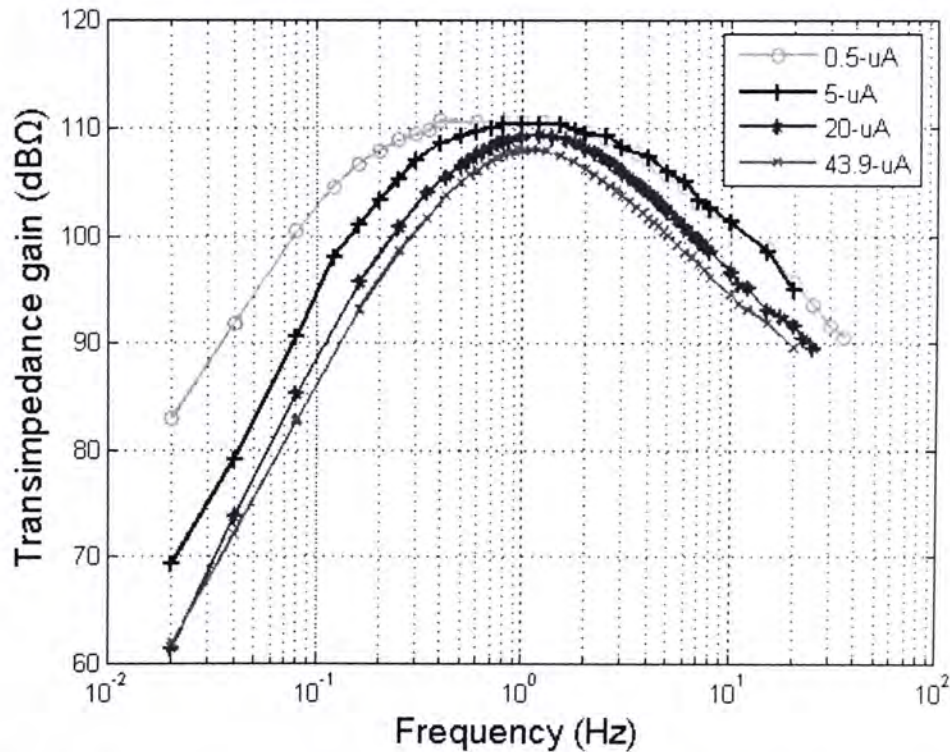


Fig. 4.15 Frequency response of overall system. With $I_{dc} = 6 \mu\text{A}$ and $I_{uc} = 1.08 \mu\text{A}$. $f_{-3dB \text{ low}} = 0.36 \text{ Hz}$, and $f_{-3dB \text{ high}} = 6.5 \text{ Hz}$, respectively.

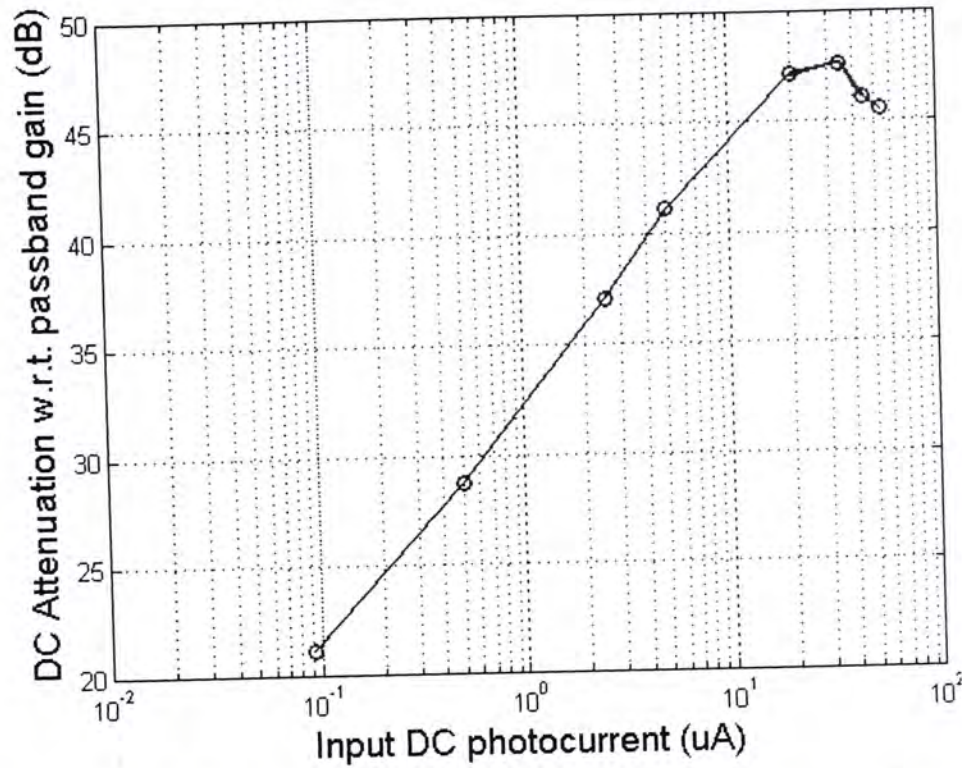


Fig. 4.16 To illustrate common-mode dynamic range of overall system. For a 20-dB attenuation, the circuit works with I_{dc} from 0.1- μ A to 53- μ A, which is about 54.5-dB!

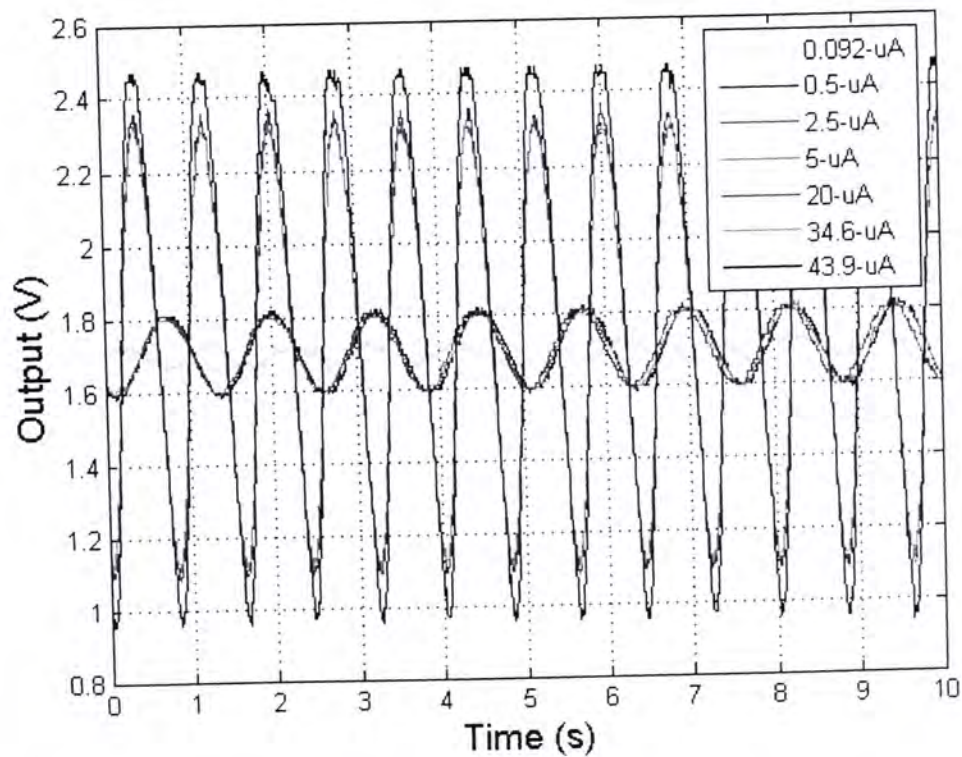


Fig. 4.17 Transient waveform of overall system with different amount of I_{dc} , to demonstrate the functionality of over all system to reject DC current.

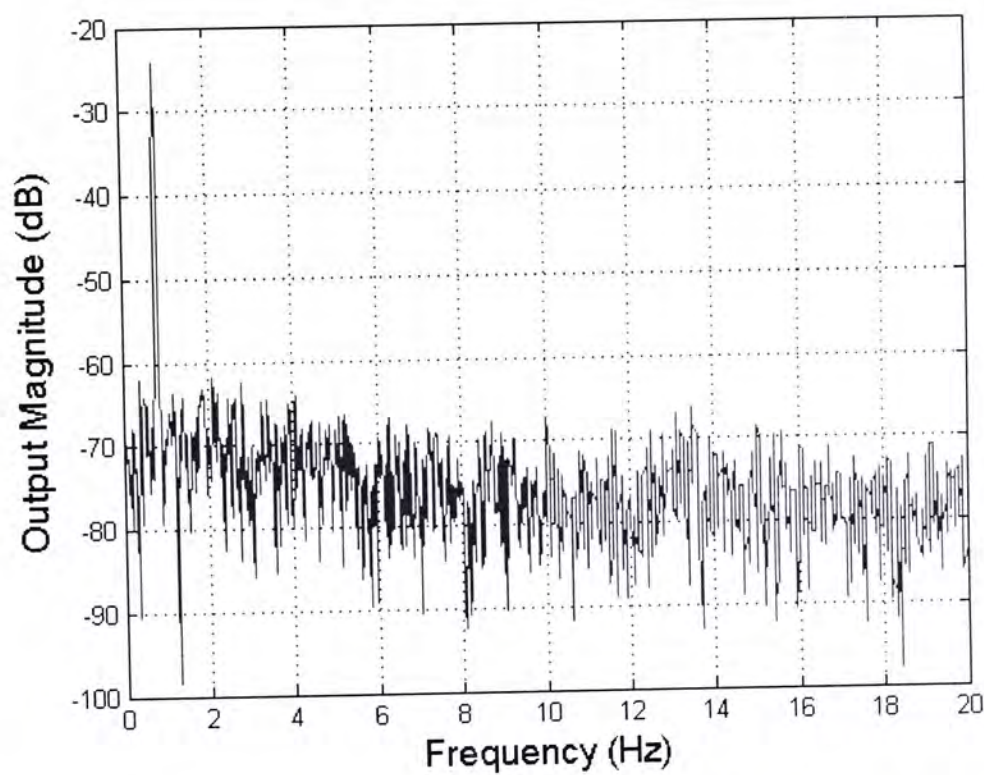


Fig. 4.18 FFT of output transient waveform at I_{dc} of 5- μ A. SFDR and SNDR are both 37.7-dB.

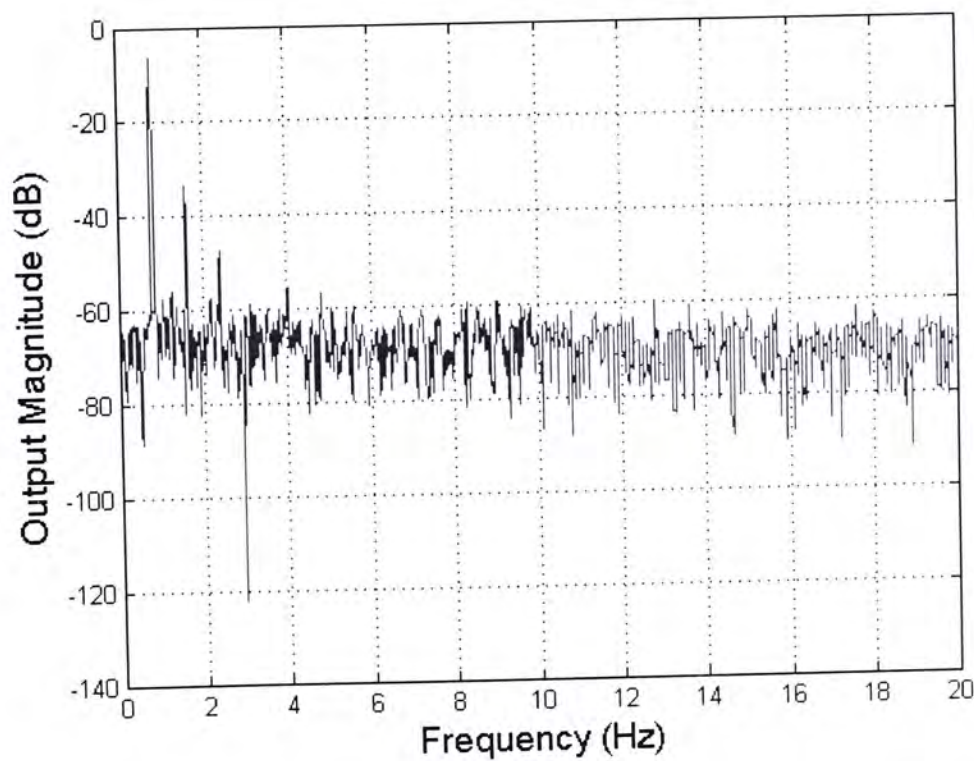


Fig. 4.19 FFT of output transient waveform at I_{dc} of 43.9- μ A. SFDR is 27-dB and SNDR is 25.3-dB.

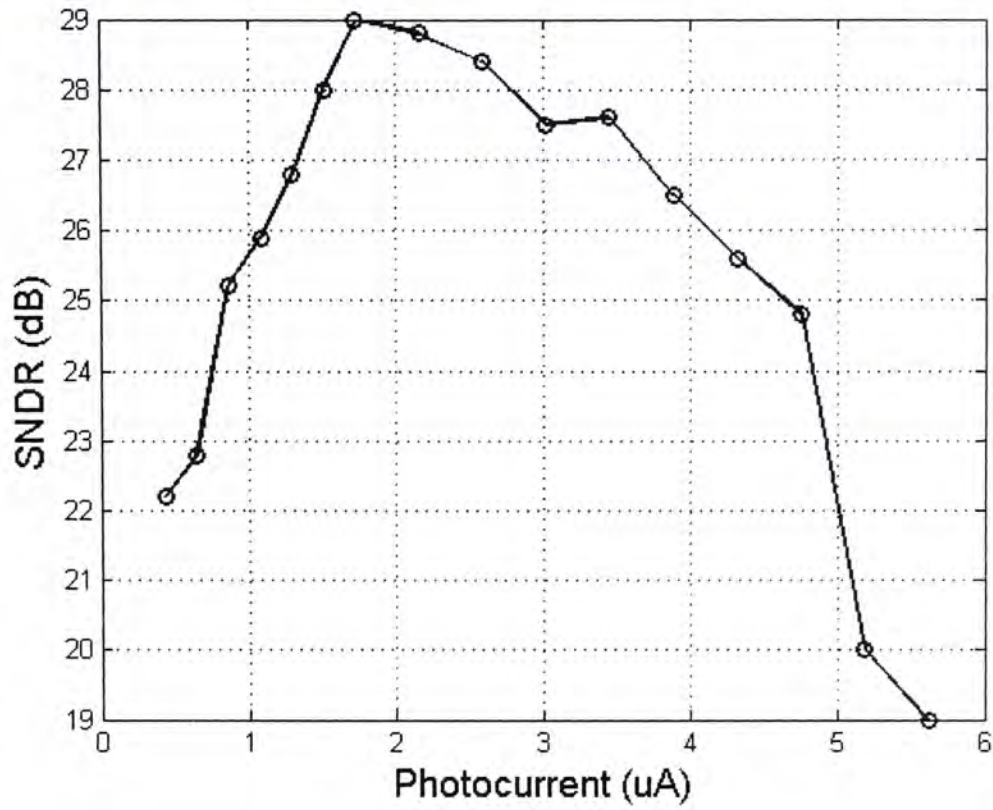


Fig. 4.20 Dynamic range overall system only. For a 21-dB SNDR ($\sim 5\%$ THD), the DR is about 29.8-dB. $I_{dc} = 3 \mu\text{A}$.

The start up transient is shown in Fig. 4.21, which is taken at the output of the CS-LPF when the finger is placed onto the sensor unit. As the finger is placed onto the sensor, the system is excited and hence the overshoot, after which the feedback loop kicks in to perform DC photocurrent rejection. This matches that of Fig. 3.29 in the previous chapter – the settling time of the circuit is about 1.68-s. Fig. 4.22 is the captured image from the oscilloscope at the output of CS-LPF, which displays the actual PPG signal as it settles. The overall system (TIA, amplifier and CS-LPF) is clearly working as distinguished features of the PPG signal can be noted (dichromatic notch, peak, etc.) and the signal settles at about 1.77-V.

Fig. 4.23 shows the PPG waveform taken at the output of the system for 12 different subjects to demonstrate consistency and functionality of entire system. Clearly, the circuit is working as all output settles to about 1.77-V. Accordingly, the proposed circuit can remove the DC offset properly and hence increases DR of the system. The performance of the PPG AFE is recapped in Table 4.3 and the comparison with previous works is shown in Table 4.4.

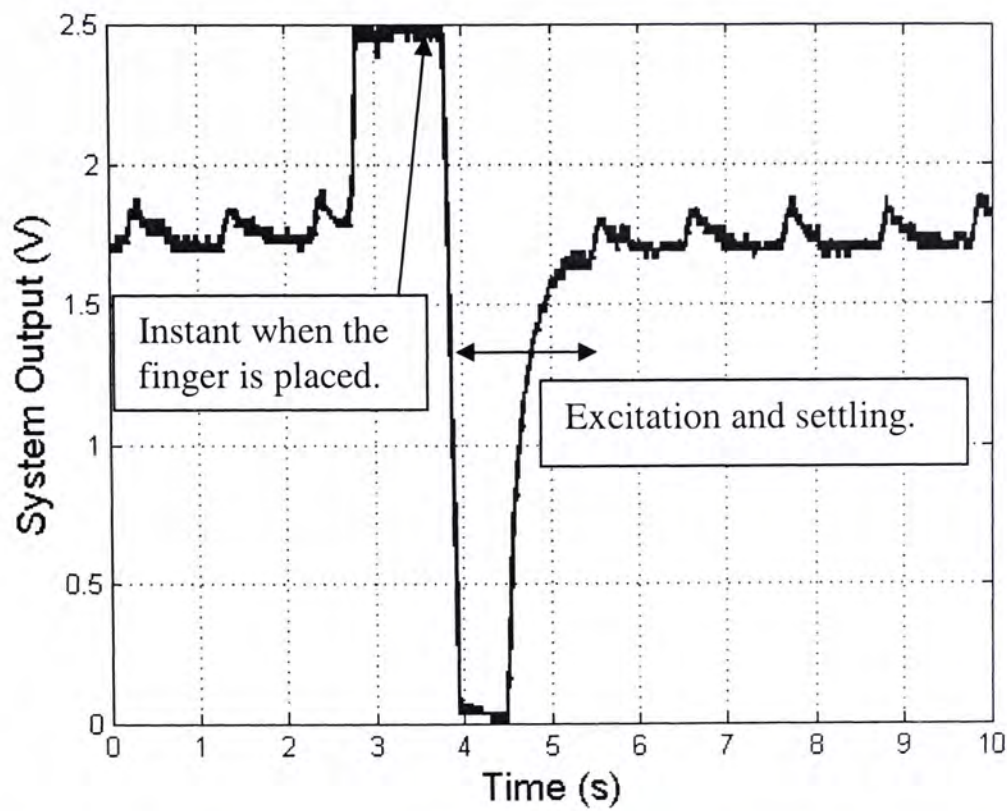


Fig. 4.21 Transient response of the circuit during start-up; this is taken at the output of CS-LPF.

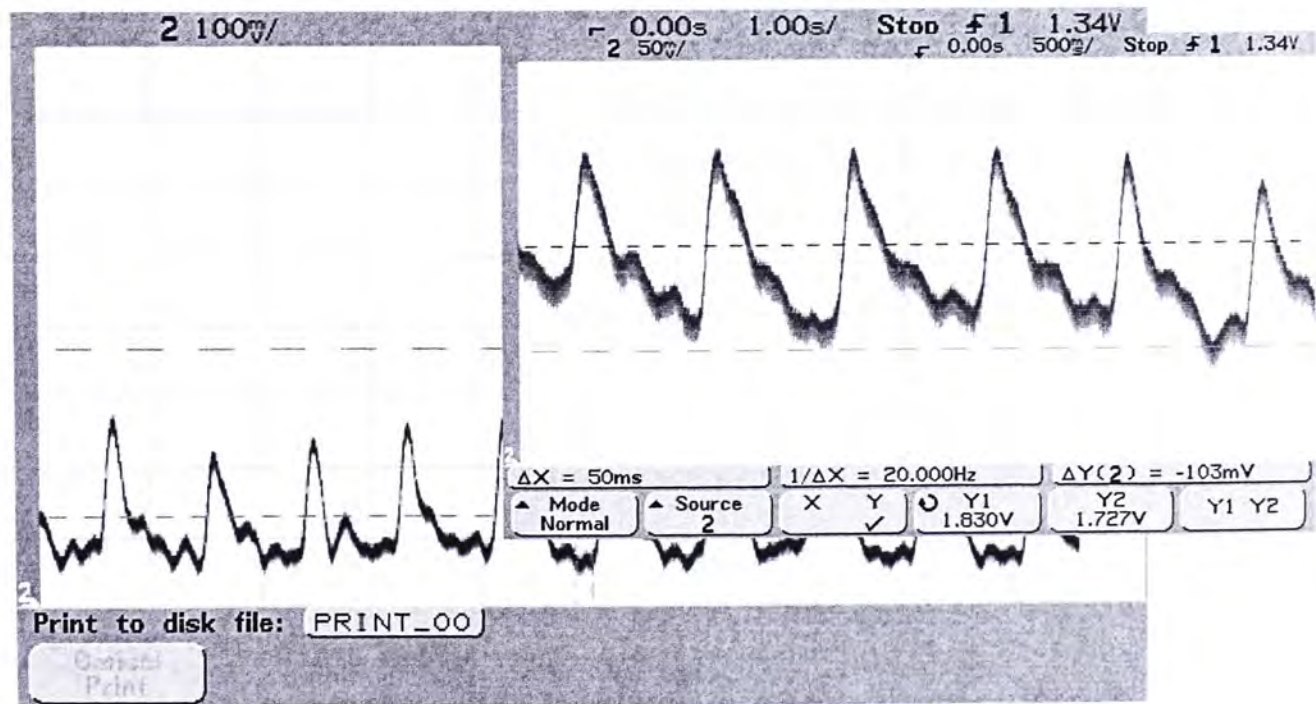


Fig. 4.22 Transient waveform taken at the output of CS-LPF. Inset: zoom in waveform of transient figure. It settles at 1.77-V.

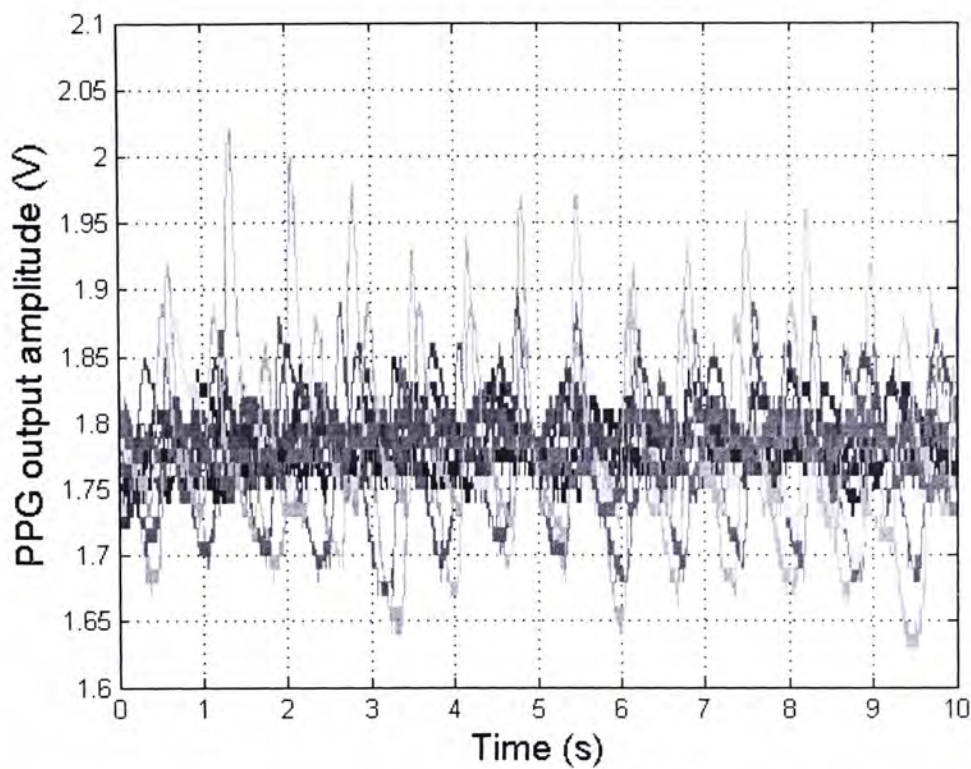


Fig. 4.23 PPG of 12 subjects to demonstrate consistency and functionality of the entire system.

Technology	4M/2P 0.35- μ m CMOS
Supply voltage	2.5-V
Power consumption	0.6-mW
Frequency cutoff	0.6-Hz (lower band) 1.8-Hz – 62-Hz (upper band)
THD/SNDR	37.7-dB
Dynamic range	29.8-dB
Core area	0.55-mm ²

Table 4.3 Performance of the PPG signal processing chain.

Ref	V_{supply}	f_{cutoff}	Current (A)	Input referred Noise (V / $\sqrt{\text{Hz}}$)	DR (THD)	THD (v_{in})	SNDR (dB)
[10]	1.8	0.3 - 50 K	166 μ (TIA)	2.2 nA (input integrated)	-	-	-
[23]	1.0-V – 1.8-V	8 - 30	3 μ	-	-	0.3% (10m)	42.6
[37]	2.65-V	0.474 - 31.5	179.5 μ	8 μ @ 30 Hz	-	-	-
[38]	± 1.5 -V	0.3 - 150	485 μ	0.86 μ	-	-	71 (SFDR)
[39]	± 2.5 -V	250	340 u	-	-	0.3%	73 (SNR)
This work	2.5-V	0.5 – 6.5	240 μ	1.2 nA @ 4 Hz, 3.53 nA (input integrated)	33.6 dB (5%)	1.4%	34.6

Table 4.4 Comparison of the PPG signal processing chain with previous works.

4.3 Summary

An ultra-low cutoff frequency filter and the entire PPG signal processing chain fabricated in 0.35- μm CMOS technology were presented in this chapter. The ultra-low cutoff frequency filter was implemented using CST to steer partial AC current to ground so as to increase the effective capacitance. It achieves a lowpass f_{-3dB} that ranges from 1.57-Hz to 58.2-Hz. The circuit works properly as the measurement results have shown. The lowpass filter consumes 78.9- μW from a 2.5-V supply and has a DR of 54.5-dB. As shown from Table 4.2, this filter is the first ultra-low cutoff frequency filter ever reported using active-RC implementation with reasonable noise and DR.

Then this lowpass filter is realized as part of the PPG signal processing chain, together with the off-chip capacitor TIA reported in Chapter 3. The entire system can reject DC current from 0.1- μA to 53- μA , which translates to LED duty cycle from 0.2 percent to 70 percent. Then experimental results demonstrate the functionality and consistency of the system with a 12-subject test, in which their waveforms all settle to 1.77-V in 1.68-s. In addition, the distinctive features of the PPG signal can be noted as well. The entire system achieves lower-band and upper-band f_{-3dB} from

0.46-Hz to 2.8-Hz and consumes 600- μ W from a 2.5-V with $I_{dc} = 6 \mu\text{A}$ (at 10% duty cycle, full power = 60 μA). Compared to other previously designed system, the performance of this is only mediocre. Nonetheless, this is the first ever designed analog front-end for bio-optical sensing application (PPG) and it can be improved significantly in the near future.

CHAPTER 5: CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

In this thesis, a new NIR sensing system for PPG signal acquisition and a new dual-loop transimpedance amplifier (TIA) for versatile physiological signal acquisition, which can be used together with ECG signal as the analog front-end for a continuous-time blood pressure monitor, have been presented. With its wide range of frequency tuning through varying the input DC current, the front-end can also be employed in neural-photonics sensing and hearing-aid application.

The NIR sensing system for PPG signal acquisition consists of a transimpedance front-end with DC rejection and an ultra-low cutoff frequency lowpass filter using current-steering technique. Light source is pulsed to reduce the power consumption. The transimpedance front-end for this signal processing chain employs a sample-and-hold in the feed-forward path to sense the DC level of the pulsed signal from the photodiode, and an error-amplifier in the feedback path with an off-chip compensation capacitor to reject the undesired DC photocurrent, which will reduce the dynamic range of the system if not rejected properly. A new technique for ultra-low cutoff frequency lowpass filter is also developed which incorporates a pair of current steering transistors to increase the effective value of the filter capacitor. The design was realized in 0.35- μm CMOS technology. It consumes 600- μW at 2.5-V, and achieves a lower and upper -3dB cutoff frequencies of 0.46-Hz and 2.8-Hz respectively. The author's contributions in this design include 1) identifying the nature of incoming signal, which includes its variable DC characteristic due to LED sampling frequency and duty cycle, and physiological condition of the individuals, 2) identifying the key issues associated with pulsed signal sensing and 3) devising a solution for it.

To achieve full integration and versatility, a novel dual-loop TIA with DC photocurrent rejection for continuous-time multi-parameter processing has been developed. It consists of a pole location control block and a self-regulated DC photocurrent rejection loop. Low frequency operation is achieved with the addition of transconductance and transimpedance elements to push the lower -3dB cutoff frequency to low frequency location. The DC current rejection loop senses the DC

current from the photodiode and performs cancellation. The design was fabricated in 0.35- μm CMOS technology. Experimental results show that the circuit can reject DC current from 2.5- μA to 110- μA , and achieves a lower -3dB cutoff frequency from 0.47-Hz to 372-Hz without any external components, which corresponds to a 443.6 times reduction in capacitor size. It consumes 156- μW and 109- μW from a 2.5-V and 2.0-V supplies at $I_{dc} = 20 \mu\text{A}$, respectively.

To analyze such a complicated circuit would require the use of special technique. Not only does this thesis contribute novel circuits to tackle the problem, it also provides insight to circuit design through DPI/SFG, which greatly expedites, enhances and adds understanding to the design process.

5.2 Future work

Numerous issues can be pursued in the future for this area, which includes the following:

1. Fully integrated front-end for PPG signal processing – which is basically combining the first and second idea, by adding a sample-hold circuit to the dual-loop transimpedance amplifier, and the peripheral circuit, such as lowpass filter, timer, oscillators and ADCs, etc. The quality of the sample-hold would determine the THD and SNDR of the overall system.
2. Low voltage transimpedance amplifier with DC photocurrent rejection – since three components are stacked (two transistors plus photodiode) together in the DC current rejection loop; this topology would not work for low voltage operation – this is the bottleneck. If the loop can be removed, there needs to be a way to perform current cancellation and pole lowering operation simultaneously. That task would inevitably rest with the error amplifier. Therefore, effort should be directed to the design of error amplifier with large compensation capacitor and techniques for frequency compensation should be developed that results in capacitance multiplication.
3. Ultra-low cutoff frequency filter design – current-steering technique should be further investigated such that it can be used for high-pass filtering or for the purpose of capacitance multiplication.

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APPENDIX A – DETAILS ABOUT THE OPERATION

% TIA with ambient photocurrent rejection loop with no Gmx. %--- the

% correct one (full version).

%

% % I = 1uA

% %

% Cp1 = 348.6e-15; Cp2 = 5e-12; Cm = 164.8e-12; Cl1 = 1e-12; Cf = 5e-12;

% Cp4 = 122.7e-15; Cp5 = 5e-12; Cp6 = 26.9e-15; Cp7 = 1.121e-12;

%

% R02 = 170.3e9; R01 = 100e3; Rf = 2.0e3;

% Av1 = 10000; Av2 = 342.76e3;

%

% Gm1 = 319.2e-9; Gm2 = 106.3e-9; Gm3 = 26.37e-6; Gmb3 = 6.253e-6;

% Gm4 = 2.471e-6; Gmb4 = .5866e-6; Gm5 = 2.188e-6; Gm6 = 4.281e-6;

% Gm7 = 4.051e-6; Gm8 = 63.2e-9; Gmctl = 25.7e-6;

% I = 5uA

%

Cp1 = 2.0655e-12; Cp2 = 5e-12; Cm = 164.8e-12; Cl1 = 1e-12; Cf = 5e-12;

Cp4 = 180.9e-15; Cp5 = 5e-12; Cp6 = 111.4e-15; Cp7 = 3.867e-12;

R02 = 59.7e9; R01 = 100e3; Rf = 2.0e3;

Av1 = 10000; Av2 = 120.22e3;

Gm1 = 1.156e-6; Gm2 = 217.2e-9; Gm3 = 121.3e-6; Gmb3 = 28.6e-6;

Gm4 = 11.28e-6; Gmb4 = 2.663e-6; Gm5 = 9.765e-6; Gm6 = 19.05e-6;

Gm7 = 16.39e-6; Gm8 = 253.4e-9; Gmctl = 93.12e-6;

% % I = 30uA

% %

% Cp1 = 2.045e-12; Cp2 = 5e-12; Cm = 164.8e-12; Cl1 = 1e-12; Cf = 5e-12;

% Cp4 = 552.5e-15; Cp5 = 5e-12; Cp6 = 403e-15; Cp7 = 7.19e-12;

%

% R02 = 161.2e9; R01 = 100e3; Rf = 2.0e3;

% Av1 = 10000; Av2 = 324.5e3;

%

% Gm1 = 4.126e-6; Gm2 = 757.5e-9; Gm3 = 632.4e-6; Gmb3 = 152.8e-6;

% Gm4 = 58.45e-6; Gmb4 = 14.1e-6; Gm5 = 45.29e-6; Gm6 = 88.03e-6;

% Gm7 = 56.1e-6; Gm8 = 854.8e-9; Gmctl = 331.8e-6;

% % I = 90uA

% %

% Cp1 = 2.096e-12; Cp2 = 5e-12; Cm = 164.8e-12; Cl1 = 1e-12; Cf = 5e-12;

% Cp4 = 1.005e-12; Cp5 = 5e-12; Cp6 = 499.5e-15; Cp7 = 7.254e-12;

%

% R02 = 86.3e9; R01 = 100e3; Rf = 2.0e3;

% Av1 = 10000; Av2 = 173.8e3;

%

% Gm1 = 7.525e-6; Gm2 = 838.3e-9; Gm3 = 1.592e-3; Gmb3 = 388.1e-6;

% Gm4 = 146.4e-6; Gmb4 = 35.7e-6; Gm5 = 98.1e-6; Gm6 = 190.1e-6;

% Gm7 = 99.89e-6; Gm8 = 1.515e-6; Gmctl = 604.3e-6;

Gm3t = Gm3+Gmb3;

```

G157 = Gm1*Gm5*Gm7;
G4T68CTL = (Gm4+Gmb4)*Gm6*Gm8*Gmctl;
C7G1G5 = Cp7*Gm1*Gm5;
G7C1G5 = Gm7*Cp1*Gm5;
C7C1G5 = Cp7*Cp1*Gm5;

% Zeroes
%_
%_

z1 = 1/(2*pi*R02*Cm)
% z2 =
(Gm1*(Gm3+Gmb3)*Gm5*Gm7*(Gm3+Gmb3+1/Rf)-(Gm4+Gmb4)*Gm6*Gm8*Gmctl*(Gm3+Gmb3+1/Rf))/
(2*pi*(Gm1*(Gm3+Gmb3)*Gm5*Cp7*(Gm3+Gmb3+1/Rf)+Gm1*Gm5*Gm7*(Gm3+Gmb3+1/Rf)*(Cp5+Cp4)-
(Gm4+Gmb4)*Gm6*Gm8*Gmctl*Cp4))
% z2b =
((1/Rf+Gm3t)*G157*Gm3t-G4T68CTL*Gm3t)/(2*pi*(Gm3t*(1/Rf+Gm3t)*(G7C1G5+C7C1G5)-G4T68CTL*Cp4))

z2 = Gm1*G157*(Gm3t*G157-G4T68CTL) /
(2*pi*(Cp1*(Gm3t*G157-G4T68CTL)*G157+Gm1*(G7C1G5+C7G1G5)*(2*Gm3t*G157-G4T68CTL))
)

% % z2a =
((Gm4+Gmb4)*Gm6*Gm8*Gmctl*(Gm3+Gmb3+1/Rf)-Gm1*(Gm3+Gmb3)*Gm5*Gm7*(Gm3+Gmb3+1/Rf))/
(2*pi*((Gm4+Gmb4)*Gm6*Gm8*Gmctl*Cp4-Gm5*(Gm1*(Gm3+Gmb3)*Cp7*(Gm3+Gmb3+1/Rf)+Gm1*Gm7*(Cf*(Gm3+Gmb3+1/Rf)+Cp5*(Gm3+Gmb3+1/Rf))))

% Poles
%_
%_

p1 = Av2*Rf*Gm2*Gmctl/(2*pi*R02*Cm*Gm1)
% p2 = 1/(2*pi*(1/Gm7)*Cp7)
p2 = sqrt((G157+G4T68CTL*Rf)*G157*Gm1 /
(G157*(2*Cp1*C7G1G5+Gm7*(Cp1^2)*Gm5)+(G7C1G5+C7G1G5)*(2*Cp1*G157+Cp7*(Gm1^2)*Gm5+Cp1*G4T68CTL*Rf)+Gm1*(G157+G4T68CTL*Rf)*(C7C1G5+((Cf+C1l)*Rf+(Cf+Cp4)*Rf/(1+Gm3t*Rf))*(G7C1G5+C7G1G5))))
p4 = 1/(2*pi*Rf*Cf)

% Numerator
%_
%_

b2 =
0.5*Cm*R02*((1/Rf+(Gm3+Gmb3))^2)*(Gm3+Gmb3)*(Av1/R01)*(Cp1*((Gm3+Gmb3)*G157-G4T68CTL)*G157+Gm1*(G7C1G5+C7G1G5)*(2*(Gm3+Gmb3)*G157-G4T68CTL));
b1 =
0.5*Cm*R02*Gm1*G157*(Gm3+Gmb3)*(Av1/R01)*(((Gm3+Gmb3)+1/Rf)^2)*((Gm3+Gmb3)*G157-G4T68CTL);
b0 =
0.5*Gm1*G157*(Gm3+Gmb3)*(Av1/R01)*(((Gm3+Gmb3)+1/Rf)^2)*((Gm3+Gmb3)*G157-G4T68CTL);

% Denominator
%_
%_

a3 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(Cm*R02*Av1/R01)*(G157*(2*Cp1*C7G1G5+Gm7*(Cp1^2)*Gm5)+(G7C1G5+C7G1G5)*(2*Cp1*G157+Cp7*(Gm1^2)*Gm5+Cp1*G4T68CTL*Rf)+Gm1*(G157+G4T68CTL*

```



```

Rf)*(C7C1G5+((Cf+Cl1)*Rf+(Cf+Cp4)*Rf/(1+Gm3t*Rf))*(G7C1G5+C7G1G5)));

a2 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(Cm*R02*Av1/R01)*(G157*(2*Cp1*G157+Cp1*G4T68CTL*Rf+Cp7*(G
m1^2)*Gm5)+Gm1*(G7C1G5+C7G1G5)*(G157+G4T68CTL*Rf));

a1 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(G157+G4T68CTL*Rf)*(Av1/R01)*((G7C1G5+C7G1G5)*(Gmct1*Gm2*
Av2*Rf)+G157*Cm*R02*Gm1);

a0 = ((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(G157+G4T68CTL*Rf)*(G157*Gmct1*Gm2*Av1*Av2*Rf/R01);

filter_function = tf([b2 b1 b0],[a3 a2 a1 a0]);
Np=500;
f=logspace(-3,12,Np);
[mag,phase] = bode(filter_function, f);
magdb = 20*log10(mag);

for i=1:length(magdb)

    test(i)=magdb(i);

end

freq_hz = f / (2*pi);

ppg_sim1=load('C:\Documents and Settings\Alex My
Documents\work\cas\transia_only\data\2p5V_ac_5uA_model.txt');
freq_sim1 = ((ppg_sim1(:,1')));
dB_sim1 = 20*log10(ppg_sim1(:,2));

figure(1);
subplot(4,1,4); semilogx (freq_hz,test,freq_sim1,dB_sim1,'-'); axis([0.001 1.659e5 -40 80]); hold on;
% legend ('analytical','simulated')
% xlabel('Frequency (Hz)');
% ylabel('Output (dB)');
zero(filter_function)
pole(filter_function)

```

APPENDIX B – COMPLEX POLE DERIVATION

$$D(s) = a_3 \left(s^3 + \frac{a_2}{a_3} s^2 + \frac{a_1}{a_3} s + \frac{a_0}{a_3} \right) = a_3 (s + \omega_{p1}) \left(s^2 + \frac{\omega_o}{Q} s + \omega_o^2 \right)$$

$$\therefore s \left(\frac{\omega_o}{Q} \omega_{p1} + \omega_o^2 \right) = \frac{a_1}{a_3} s, \text{ and } s^2 \left(\frac{\omega_o}{Q} + \omega_{p1} \right) = \frac{a_2}{a_3} s^2$$

$$\frac{\omega_o}{Q} \omega_{p1} + \omega_o^2 = \frac{a_1}{a_3} = \frac{\omega_o \omega_{p1} + \omega_o^2 Q}{Q}$$

$$a_3 = \frac{a_1 Q}{\omega_o \omega_{p1} + \omega_o^2 Q} \quad (1)$$

On the otherhand,

$$\frac{\omega_o}{Q} + \omega_{p1} = \frac{a_2}{a_3} = \frac{\omega_o + \omega_{p1} Q}{Q}$$

$$a_3 = \frac{a_2 Q}{\omega_o + \omega_{p1} Q} \quad (2)$$

We can equate (1) and (2)

$$\frac{a_1}{\omega_o \omega_{p1} + \omega_o^2 Q} = \frac{a_2}{\omega_o + \omega_{p1} Q}$$

$$a_1 (\omega_o + \omega_{p1} Q) = a_2 (\omega_o \omega_{p1} + \omega_o^2 Q)$$

$$a_1 \omega_o + a_1 \omega_{p1} Q = a_2 \omega_o \omega_{p1} + a_2 \omega_o^2 Q$$

$$a_1 \omega_o - a_2 \omega_o \omega_{p1} = (a_2 \omega_o^2 - a_1 \omega_{p1}) Q$$

$$Q = \frac{a_1 \omega_o - a_2 \omega_o \omega_{p1}}{a_2 \omega_o^2 - a_1 \omega_{p1}}$$

Q is preferably to be small to reduce peaking and $\omega_o \gg \omega_{p1}$.

APPENDIX C – DETAILS ABOUT NOISE DERIVATION

% TIA with ambient photocurrent rejection loop with no Gmx. % the
% correct one (full version).
%

% % I = 5uA
% %
% Cp1 = 2.0655e-12; Cp2 = 5e-12; Cm = 164.8e-12; Cll = 1e-12; Cf = 5e-12;
% Cp4 = 180.9e-15; Cp5 = 5e-12; Cp6 = 111.4e-15; Cp7 = 3.867e-12;
%
% R02 = 59.7e9; R01 = 100e3; Rf = 2.0e3;
% Av1 = 10000; Av2 = 120.22e3;
%
% Gm1 = 1.156e-6; Gm2 = 217.2e-9; Gm3 = 121.3e-6; Gmb3 = 28.6e-6;
% Gm4 = 11.28e-6; Gmb4 = 2.663e-6; Gm5 = 9.765e-6; Gm6 = 19.05e-6;
% Gm7 = 16.39e-6; Gm8 = 253.4e-9; Gmctl = 93.12e-6;

% I = 30uA
%
Cp1 = 2.045e-12; Cp2 = 5e-12; Cm = 164.8e-12; Cll = 1e-12; Cf = 5e-12;
Cp4 = 552.5e-15; Cp5 = 5e-12; Cp6 = 403e-15; Cp7 = 7.19e-12;

R02 = 161.2e9; R01 = 100e3; Rf = 2.0e3;
Av1 = 10000; Av2 = 324.5e3;

Gm1 = 4.126e-6; Gm2 = 757.5e-9; Gm3 = 632.4e-6; Gmb3 = 152.8e-6;
Gm4 = 58.45e-6; Gmb4 = 14.1e-6; Gm5 = 45.29e-6; Gm6 = 88.03e-6;
Gm7 = 56.1e-6; Gm8 = 854.8e-9; Gmctl = 331.8e-6;

% % I = 90uA
% %
% Cp1 = 2.096e-12; Cp2 = 5e-12; Cm = 164.8e-12; Cll = 1e-12; Cf = 5e-12;
% Cp4 = 1.005e-12; Cp5 = 5e-12; Cp6 = 499.5e-15; Cp7 = 7.254e-12;
%
% R02 = 86.3e9; R01 = 100e3; Rf = 2.0e3;
% Av1 = 10000; Av2 = 173.8e3;
%
% Gm1 = 7.525e-6; Gm2 = 838.3e-9; Gm3 = 1.592e-3; Gmb3 = 388.1e-6;
% Gm4 = 146.4e-6; Gmb4 = 35.7e-6; Gm5 = 98.1e-6; Gm6 = 190.1e-6;
% Gm7 = 99.89e-6; Gm8 = 1.515e-6; Gmctl = 604.3e-6;

Gm3t = Gm3+Gmb3;
Gm4t = Gm4+Gmb4;
G157 = Gm1*Gm5*Gm7;
G4T68CTL = (Gm4+Gmb4)*Gm6*Gm8*Gmctl;
G468CTL = (Gm4)*Gm6*Gm8*Gmctl;
G4T68 = (Gm4+Gmb4)*Gm6*Gm8;
C7G1G5 = Cp7*Gm1*Gm5;
G7C1G5 = Gm7*Cp1*Gm5;
C7C1G5 = Cp7*Cp1*Gm5;

% noise calculation

%

```
Np=100;
f=logspace(0,7,Np);
% f = [1:10e6];
Kn = 5.1e-27;
Kp = 8.5e-27;
Cox = 4.54e-15;
w=2*pi*f;
W3 = 280.5; L3 = 1.2;
Wctl = 200; Lctl = 4;
W4 = 25.5; L4 = 1.2;
W5 = 34; L5 = 2;
W6 = 64.6; L6 = 2;
W7 = 320; L7 = 120;
W1 = 2.5; L1 = 4;
W2 = 0.5; L2 = 90;
W8 = 5; L8 = 120;
lamp2_sq = 1e-21;
lamp1_sq = 1e-28;
% lamp2_sq = 0;
InRf_sq = 4*1.38e-23*300/Rf;

bx1 = (1-G4T68CTL/(Gm3t*G157))/(1-(Gm3t/(Gm3t+1/Rf))*(1-G4T68CTL/(Gm3t*G157)));
bx2 = (1/(Gm3t+1/Rf))/(1-(Av1/R01)*(1/(Gm3t+1/Rf)));
bx5 = (Gm3t*G157-G4T68CTL)/(Gm3t*(G157/Rf+G4T68CTL));
```

% Noise contribution by each transistor

%

for i=1:Np

% noise of M3

%

% $In3_sq = 4*1.38e-23*300*(2/3)*(Gm3) + (Gm3^2)*Kn/(W3*L3*Cox*f);$

%

% $Inctl_sq = 4*1.38e-23*300*(2/3)*Gmctl + (Gmctl^2)*Kp/(Wctl*Lctl*Cox*f);$

%

% $In4_sq = 4*1.38e-23*300*(2/3)*(Gm4) + (Gm4^2)*Kn/(W4*L4*Cox*f);$

%

% $In5_sq = 4*1.38e-23*300*(2/3)*Gm5 + (Gm5^2)*Kp/(W5*L5*Cox*f);$

%

% $In6_sq = 4*1.38e-23*300*(2/3)*Gm6 + (Gm6^2)*Kp/(W6*L6*Cox*f);$

%

% $In7_sq = 4*1.38e-23*300*(2/3)*Gm7 + (Gm7^2)*Kn/(W7*L7*Cox*f);$

%

% $In1_sq = 4*1.38e-23*300*(2/3)*Gm1 + (Gm1^2)*Kp/(W1*L1*Cox*f);$

%

% $In2_sq = 4*1.38e-23*300*(2/3)*Gm2 + (Gm2^2)*Kn/(W2*L2*Cox*f);$

%

% $In8_sq = 4*1.38e-23*300*(2/3)*Gm8 + (Gm8^2)*Kn/(W8*L8*Cox*f);$

$$\text{In3in_sq}(i) = ((w(i)*Av1*Rf*R02*Cm*Gm1)^2 + (Gm2*Av1*Av2*Gmctl*(Rf^2))^2) * (4*1.38e-23*300*(2/3)*(Gm3) + (Gm3^2)*Kn / (W3*L3*Cox*w(i)/(2*pi))) / ((bx1*w(i)*Cm*Gm1*Rf*R02*R01*(1/Rf+Gm3t))^2);$$

$$\text{Inctlin_sq}(i) = ((w(i)*Av1*Rf*R02*Cm*Gm1)^2 + (Gm2*Av1*Av2*Gmctl*(Rf^2))^2) * (4*1.38e-23*300*(2/3)*Gmctl + (Gmctl^2)*Kp / (Wctl*Lctl*Cox*w(i)/(2*pi))) / ((bx1*w(i)*Cm*Gm1*Rf*R02*R01*(1/Rf+Gm3t))^2);$$

$$\text{Iamp1in_sq}(i) = ((w(i)*Av1*Rf*R02*Cm*Gm1)^2 + (Gm2*Av1*Av2*Gmctl*(Rf^2))^2) * (\text{Iamp1_sq}) / ((bx1*w(i)*Cm*Gm1*Rf*R02*R01*(1/Rf+Gm3t))^2);$$

$$\text{In4in_sq}(i) = ((w(i)*G157*R01*R02*Cm*Gm1*Gm3t)^2 - (Gm2*Av1*Av2*Rf*Gmctl*Gm3t*G157*bx2)^2) * (4*1.38e-23*300*(2/3)*(Gm4) + (Gm4^2)*Kn / (W4*L4*Cox*w(i)/(2*pi))) / ((w(i)*G157*R01*R02*Cm*Gm1*Gm4t)^2 - (Gm2*Av1*Av2*Rf*Gmctl*Gm4t*G157*bx2)^2);$$

$$\text{In5in_sq}(i) = ((w(i)*G157*R01*R02*Cm*Gm1*Gm3t)^2 - (Gm2*Av1*Av2*Rf*Gmctl*Gm3t*G157*bx2)^2) * (4*1.38e-23*300*(2/3)*Gm5 + (Gm5^2)*Kp / (W5*L5*Cox*w(i)/(2*pi))) / ((w(i)*G157*R01*R02*Cm*Gm1*Gm4t)^2 - (Gm2*Av1*Av2*Rf*Gmctl*Gm4t*G157*bx2)^2);$$

$$\text{In6in_sq}(i) = ((Gm5*Gm3t/(Gm4t*Gm6))^2) * (4*1.38e-23*300*(2/3)*Gm6 + (Gm6^2)*Kp / (W6*L6*Cox*w(i)/(2*pi)));$$

$$\text{In7in_sq}(i) = ((Gm5*Gm3t/(Gm4t*Gm6))^2) * (4*1.38e-23*300*(2/3)*Gm7 + (Gm7^2)*Kn / (W7*L7*Cox*w(i)/(2*pi)));$$

$$\text{In1in_sq}(i) = ((w(i)*Gm3t*Gm5*Gm7*G157*R01*R02*Cm*Gm1)^2 - (Gm3t*Gm5*Gm7*Gm2*Av1*Av2*Rf*Gmctl*G157*bx2)^2) * (4*1.38e-23*300*(2/3)*Gm1 + (Gm1^2)*Kp / (W1*L1*Cox*w(i)/(2*pi))) / ((w(i)*G4T68*G157*R01*R02*Cm*Gm1)^2 - (G4T68*G157*Gm2*Av1*Av2*Rf*Gmctl*bx2)^2);$$

$$\text{In2in_sq}(i) = ((w(i)*Gm3t*Gm5*Gm7*G157*R01*R02*Cm*Gm1)^2 - (Gm3t*Gm5*Gm7*Gm2*Av1*Av2*Rf*Gmctl*G157*bx2)^2) * (4*1.38e-23*300*(2/3)*Gm2 + (Gm2^2)*Kn / (W2*L2*Cox*w(i)/(2*pi))) / ((w(i)*G4T68*G157*R01*R02*Cm*Gm1)^2 - (G4T68*G157*Gm2*Av1*Av2*Rf*Gmctl*bx2)^2);$$

$$\text{In8in_sq}(i) = ((w(i)*Gm3t*Gm5*Gm7*G157*R01*R02*Cm*Gm1)^2 - (Gm3t*Gm5*Gm7*Gm2*Av1*Av2*Rf*Gmctl*G157*bx2)^2) * (4*1.38e-23*300*(2/3)*Gm8 + (Gm8^2)*Kn / (W8*L8*Cox*w(i)/(2*pi))) / ((w(i)*G4T68*G157*R01*R02*Cm*Gm1)^2 - (G4T68*G157*Gm2*Av1*Av2*Rf*Gmctl*bx2)^2);$$

$$\text{InRfin_sq}(i) = ((w(i)*Av1*Rf*R02*Cm*Gm1*bx5*(Av1/R01))^2 + (Gm2*Gmctl*Av1*Av2*(Rf^2)*bx5*(Av1/R01))^2) * (\text{InRf_sq}) / ((w(i)*bx1*bx5*Cm*Gm1*Rf*R01*R02*(1/Rf+Gm3t)*(Av1/R01))^2);$$

$$\text{Iamp2in_sq}(i) = ((w(i)*Cm*R02*Gm1*Av1)^2 + (Gm2*Gmctl*Av1*Av2*Rf)^2) * (\text{Iamp2_sq}) / ((w(i)*bx5*Cm*Gm1*R01*R02*(1/Rf+Gm3t)*(Av1/R01))^2);$$

end

```

% hold

Intot_sq = ln3in_sq + lnctlin_sq + ln4in_sq + ln5in_sq + ln6in_sq + ln7in_sq + ln1in_sq + ln2in_sq +
ln8in_sq + lampa2in_sq + lnRfin_sq + lampa1in_sq;
% Intot_sq = ln3in_sq + lnctlin_sq + ln4in_sq + ln5in_sq + ln6in_sq + ln7in_sq + ln1in_sq + ln2in_sq +
ln8in_sq + lnRfin_sq;
figure(1);
Intot_sqrt = sqrt(Intot_sq);
loglog(f,Intot_sqrt); xlabel('Frequency (Hz)'); ylabel('Input referred noise (A/Hz^1/2)');
figure(2);
loglog(f,Intot_sq,f,ln3in_sq,'o',f,lnctlin_sq,'.',f,ln4in_sq,'x',f,ln5in_sq,'+',f,ln6in_sq,'*',f,ln7in_sq,'^',f,ln1in_sq,'s',f,ln2in_sq,'d',f,ln8in_sq,'v',f,lampa2in_sq,'<',f,lnRfin_sq,'>',f,lampa1in_sq,'p'); xlabel('Frequency (Hz)');
ylabel('Input referred noise (A^2/Hz)');
legend('tot','3','ctl','4','5','6','7','1','2','8','amp2','R_f','amp1')

%_
%_

```


APPENDIX D – DETAILS ABOUT SUB-THRESHOLD

OPERATION

* I = 2.5uA

Cp1 = 794.6e-15; Cp2 = 5e-12; Cm = 164.8e-12; Cl1 = 1e-12; Cf = 5e-12;
Cp4 = 142.2e-15; Cp5 = 5e-12; Cp6 = 57.6e-15; Cp7 = 69.56e-12;

R02 = 172.25e9; R01 = 100e3; Rf = 2.0e3;
Av1 = 10000; Av2 = 346.74e3;

Id4 = 22.34e-9; Id6 = 42.45e-9; Id8 = 1.2e-9;
Id1 = 3.24e-9; Id2 = 0.2425e-9; Id3 = 259.2e-9;

Gm1 = Id1/(-10.1*0.025); Gm2 = Id2/(11.8*0.025); Gm3 = Id3/(11.8*0.025);
Gmb3 = 0;
Gm4 = Id4/(11.8*0.025); Gmb4 = 0; Gm5 = Id4/(-10.1*0.025); Gm6 =
Id6/(-10.1*0.025);
Gm7 = Id6/(11.8*0.025); Gm8 = Id8/(11.8*0.025); Gmctl =
Id3/(-10.1*0.025);

Gm3t = Gm3+Gmb3;
G157 = Gm1*Gm5*Gm7;
G4T68CTL = (Gm4+Gmb4)*Gm6*Gm8*Gmctl;
C7G1G5 = Cp7*Gm1*Gm5;
G7C1G5 = Gm7*Cp1*Gm5;
C7C1G5 = Cp7*Cp1*Gm5;

o Zeros

z1 = 1/(2*pi*R02*Cm)
z2 = Gm1*G157*(Gm3t*G157-G4T68CTL) /
(2*pi*(Cp1*(Gm3t*G157-G4T68CTL)*G157+Gm1*(G7C1G5+C7G1G5)*(2*Gm3t*G157
-G4T68CTL)))

o Poles

p1 = Av2*Rf*Gm2*Gmctl/(2*pi*R02*Cm*Gm1)
p2 = sqrt((G157+G4T68CTL*Rf)*G157*Gm1 /
(G157*(2*Cp1*C7G1G5+Gm7*(Cp1^2)*Gm5)+(G7C1G5+C7G1G5)*(2*Cp1*G157+Cp7*
(Gm1^2)*Gm5+Cp1*G4T68CTL*Rf)+Gm1*(G157+G4T68CTL*Rf)*(C7C1G5+((Cf+Cl1)
*Rf+(Cf+Cp4)*Rf/(1+Gm3t*Rf))*(G7C1G5+C7G1G5))))
p4 = 1/(2*pi*Rf*Cf)

o Numerator

b2 =
Cm*R02*((1/Rf+(Gm3+Gmb3))^2)*(Gm3+Gmb3)*(Av1/R01)*(Cp1*((Gm3+Gmb3)*G1
57-G4T68CTL)*G157+Gm1*(G7C1G5+C7G1G5)*(2*(Gm3+Gmb3)*G157-G4T68CTL));
b1 =
Cm*R02*Gm1*G157*(Gm3+Gmb3)*(Av1/R01)*(((Gm3+Gmb3)+1/Rf)^2)*((Gm3+Gmb3
) *G157-G4T68CTL);
b0 =

```
Gm1*G157*(Gm3+Gmb3)*(Av1/R01)*(((Gm3+Gmb3)+1/Rf)^2)*(Gm3+Gmb3)*G157-
G4T68CTL);
```

```
Denominator
```

```
a3 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(Cm*R02*Av1/R01)*(G157*(2*Cp1*C7G1G5+Gm7*(C
p1^2)*Gm5)+(G7C1G5+C7G1G5)*(2*Cp1*G157+Cp7*(Gm1^2)*Gm5+Cp1*G4T68CTL*R
f)+Gm1*(G157+G4T68CTL*Rf)*(C7C1G5+((Cf+C11)*Rf+(Cf+Cp4)*Rf/(1+Gm3t*Rf
))*(G7C1G5+C7G1G5)));
```

```
a2 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(Cm*R02*Av1/R01)*(G157*(2*Cp1*G157+Cp1*G4T6
8CTL*Rf+Cp7*(Gm1^2)*Gm5)+Gm1*(G7C1G5+C7G1G5)*(G157+G4T68CTL*Rf));
```

```
a1 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(G157+G4T68CTL*Rf)*(Av1/R01)*((G7C1G5+C7G1G
5)*(Gmct1*Gm2*Av2*Rf)+G157*Cm*R02*Gm1);
```

```
a0 =
((Gm3t/Rf)^2)*(1/Rf+Gm3t)*(G157+G4T68CTL*Rf)*(G157*Gmct1*Gm2*Av1*Av2*
Rf/R01);
```

```
filter_function = tf([b2 b1 b0],[a3 a2 a1 a0]);
```

```
Np=500;
```

```
f=logspace(-3,12,Np);
```

```
[mag,phase] = bode(filter_function, f);
```

```
magdb = 20*log10(mag);
```

```
for i=1:length(magdb)
```

```
test(i)=magdb(i);
```

```
end
```


CUHK Libraries



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